Philco-Ford Corporation
Microelectronics Division
Blue Bell, Pennsylvania 19422

SECOND AND THIRD QUARTERLY PROGRESS REPORT

DEVELOPMENT OF GLASS PASSIVATION METHOD FOR SEMICONDUCTOR DEVICES FOR SATURN SYSTEM

28 SEPTEMBER 1966 TO 28 MARCH 1967

Contract No. NAS8-18048
National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama

FOREWORD

The work reported here was carried out by the Philco-Ford Microelectronics Division at its facilities in Blue Bell and Lansdale, Pennsylvania. This report covers the studies performed during the period 28 September 1966 to 28 March 1967 on Contract No. NAS8-18048.

The program is administered under the direction of M. Nowakowski of the Quality Laboratory, George C. Marshall Space Flight Center, Huntsville, Alabama. The project bears the Philco-Ford internal number R-518.

SUMMARY

During this period the materials study, design evaluation and manufacturing study were performed. The discussion of the materials study includes data from experiments performed to characterize the deposited passivating film (such as oxide charge and pinhole studies), and a detailed theoretical treatment of material requirements.

The information presented on the design study indicates that essentially the results of tests conducted on the preliminary test model were not adequate to satisfactorily measure device stability as affected by ambient contamination. This led to a more sophisticated study of the specific mechanism believed to be responsible for most device instability; namely, charge accumulation on the Si02 surface. Studies of capacitive inversion and surface-field-induced inversion were performed on a variety of bipolar products in order to select a sufficiently sensitive vehicle. Based on these studies, a revised vehicle was designed and units were fabricated for study. The results obtained on this revised vehicle demonstrate that surface-field-induced inversion is less likely to occur on units which are glassed.

During the manufacturing study consideration is being given to the various applications which could take advantage of the additional layer of glass. These applications are in addition to

the mechanical protection and the protection against ambient contaminants which are naturally afforded the metalization by the additional layer of glass. The study to date indicates that the most desirable time for the application of a glass encapsulating and passivating layer during microcircuit manufacture is while the microcircuits are still in wafer form, as opposed to glass application at a point following the assembly of the discrete chip.

The vehicle of the revised design has been shown to be sensitive to surface charge accumulation, and the manufacture of a suitable number of units for the performance evaluation program is nearing completion. A description is given of the test program which will be used to measure the reliability performance of the revised vehicles.

A brief description is given of the conventional integrated circuits, glassed according to the selected process, which are being prepared for submission to NASA.

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SECTION 1 - PURPOSE

It is the purpose of this program to conduct a series of studies leading to the selection and development of a glass passivation and encapsulation process for semiconductor elements. The improved protection will be demonstrated through the evaluation and testing of devices manufactured with the selected process.

At the conclusion of the program, a complete specification describing the encapsulation material and the process of applying it to semiconductor devices will be submitted.

SECTION 2 - MATERIAL STUDY

2.1 INTRODUCTION

Detailed discussion of the considerations involved in the selection of the glass and the manner of its application to the integrated circuit is presented in Section 4 and in the Appendix. This section discusses the experiments conducted to assess the properties of vapor plated SiO_2 to characterize it as a material capable of fulfilling the requirements discussed in the Appendix.

2.2 OXIDE CHARGE CONTENT

To add to our basic understanding of the electrical properties of the oxides which might be found on typical integrated circuits, test samples were made for C-V measurements of MOS capacitors. The application of the C-V measurement technique to the study of the charge content of the vapor plated oxide was discussed in the First Quarterly Progress Report which also included experimental data. Information about the charge content in the oxides normally found on integrated circuits is useful, for example, in the determination of how much charge density must be accumulated on the oxide surface to invert the underlying silicon.

Interpretation of the results of the C-V measurements made on the test samples was not straightforward because many of the simple oxides developed leakage, an occurrence not frequently encountered and as yet unexplained, and because the low substrate

resistivity (0.2 to 0.5 Ω-cm) resulted in a small capacitance change. Test structures are usually made of 5 Ω-cm material. The lower resistivity was chosen in this case because it was typical of the value used in one of our lines of integrated circuits.

Good thermally grown oxides have about 2×10^{11} immobile charges/cm^2, and less than 1×10^{11} mobile or trapped charges/cm^2. The results of our evaluation follow.

A. Initial or Post-Epitaxial-Growth Oxide

This was thermally grown at 1285° C to a thickness of 7000 Å. The first 35 minutes were with wet oxygen, and the last 5 minutes were with dry oxygen. For some unexplained reason, both wafers in this sample were too leaky for a precise evaluation. There appear to be at least 10^{12} mobile charges/cm^2.

B. Post-Epi Oxide and Oxide Formed During Base Deposition and Drive-In

This oxide is the same as the post-epi oxide described in A above, plus the oxide formed during a boron deposition at 1020° C from a BCl_3 source in 02, N_2 and H_2, and the oxide formed during the boron drive-in at 1087° C for 50 minutes in wet O_2 followed by 50 minutes in dry O_2. The total thickness of this oxide is about 8000 Å. These samples had 6.5×10^{11} to 10×10^{11} immobile charges/cm^2, and 4×10^{11} to 8×10^{11} mobile charges/cm^2.

C. Post-Epi Oxide, Base Oxide and Emitter Oxide

This oxide is the same as that described in B above, plus the oxide formed during the depostion and drive-in of the emitter. The source is $POCl_3$. The deposition is made in dry N_2 and dry O_2 at 1040° C for a period of 8 minutes, and the drive-in is performed at the same temperature in wet O_2 for 10 to 12 minutes. The thickness of the oxide is estimated to be 8000 Å. The immobile charge density is about 7×10^{11} cm^{-2}, and there is no measurable mobile charge.

D. Sample With Phosphorus Glass Removed

Same as C above except that 3000 Å of the phosphorus glass was etched away. This sample had about 8×10^{11} immobile charges/cm^3, and no measurable mobile charge.

E. Metalization by Tungsten Coil Evaportion

Same as C above. A layer of Al (10kÅ thick) was evaporated from a tungsten coil and alloyed at 475° C for 15 minutes. These samples had about 5.5×10^{11} immobile charges/cm^3, and no measurable mobile charge.

We considered making similar evaluation of the oxides grown on bare silicon during the diffusions, but the high density of doping atoms in a diffusion layer causes the capacitance charge to be too small. While it is unfortunate that so many of the samples were leaky and that the resistivity of the silicon was too low to get a well defined change in the C-V curve, the following conclusions can be made:

1. There appears to be a large amount (10^{12}) of mobile charge in the initial or post-epi oxide.
2. As expected, the phosphorus glass getters out the mobile ions, even when the aluminum is evaporated from a tungsten coil.
3. Removal of the 3000 Å of phosphorus glass does not seem to affect any of the charge densities in the oxide.
4. The alloying of the aluminum slightly reduces the immobile charge density.

This experiment is worth repeating if time permits. The resistivity of the silicon should be higher to yield a higher capacitance change ratio, While we do not understand why there was a leakage problem in this test, we believe that there would probably not be a leakage problem in a repeat test because we do not generally have a leakage problem.

2.3 PINHOLE STUDIES

Pinhole density is one of the important characteristics of a glass passivation layer. The factors contributing to the pinhole density of a glass layer on an integrated circuit include 1) imperfect wafer cleanliness prior to glass deposition, 2) the inherent pinhole density associated with the deposition technique, 3) the pinholes introduced by the etching step because of resist defect and 4) problems associated with glass layer deposition over a nonplanar surface.

The pinhole density resulting from defects in the photoresist is strongly dependent upon the photoresist processing. Double processing is one technique we have used to minimize the number of pinholes. In this technique, the wafers are coated with resist, the resist is exposed and developed and the glass is etched half the way through; the resist is then stripped and the process repeated, etching the glass through to the bottom metal. A typical pinhole density for a particular resist process is about 200×10^{-4} pinholes/mil^2. Double processing using this same resist process results in a pinhole density of less than 2×10^{-4} pinholes/mil^2.

To determine the pinhole density to be expected from the vapor plating of SiO_2 on an integrated circuit, tests were conducted by sandwiching the layer of glass between two layers of metal and observing electrical shorts. To determine the inherent pinhole density of the vapor plated glass and also to determine the effect which different step heights have on pinhole density, the following test was conducted.

> The initial vehicle metalization patterns were delineated in 5 kÅ, 10 kÅ and 15 kÅ thick aluminum on oxidized wafers and vapor plated with 5 kÅ, 10 kÅ and 18 kÅ thick glass layers. Aluminum was then evaporated and the metal pattern for the initial vehicle was delineated. Glass etching was done after the field plate was delineated. Control wafers, showing the pinhole characteristics of the glass itself, were made by plating 5 kÅ, 10 kÅ and 18 kÅ thick glass on 10 kÅ thick undelineated aluminum, appling field plates and etching the glass in the same manner as described above. The wafers were then tested by applying 100 V between the top metal (field plate) and the lower metal. The results are shown in Table 1. Note that shorts were detected only on those wafers where the thickness of the lower aluminum is greater than the thickness of the glass coating.

TABLE 1

PINHOLE DENSITY AS RELATED TO THICKNESS OF METALIZATION & GLASS

WAFER	ALUMINUM THICKNESS	GLASS THICKNESS (kÅ)	SHORTS	PINHOLE DENSITY ($\times 10^{-4}$ pinholes/mil^2)
A	10kÅ*	5	6	1.4
B	10kÅ*	10	1	0.2
C	10kÅ*	18	0	(0.2
D	5kÅ	5	0	(2.1
E	5kÅ	10	0	(0.9
F	5kÅ	18	0	(1.8
G	10kÅ	5	13	11.0
H	10kÅ	10	0	(2.1
I	10kÅ	18	0	(0.9
J	15kÅ	5	6	17.0
K	15kÅ	10	21	17.0
L	15kÅ	18	0	(0.9

* Control units in which the bottom metal did not have a delineated pattern.

The data in Table 1 indicate that

1. The inherent pinhole density of the glass, thicker than 5kÅ, is satisfactory for double layer metalization (Wafers A, B, and C).
2. Having glass thinner than the lower aluminum is undesirable (Wafers G, J, and K).
3. Having glass and lower aluminum of the same thickness is satisfactory (Wafers D, H, and L).
4. Having glass thicker than the lower aluminum is satisfactory (Wafers E, F, and I).

2.4 TEMPERATURE LIMITATIONS

We have found that vapor plated SiO_2 plated to a thickness of 12kÅ onto anintegrated circuit, will crack when subjected to temperatures in excess of 475° C. No cracking occurs at temperatures up to 440° C. Since header bonding or package sealing is sometimes Gone at temperatures greater than 440° C, caution must be exercised in the choice of assembly techniques.

In order to determine if glass deposited at temperatures above the usual deposition temperature of 400° C would better withstand higher temperatures, a test was performed using glass deposited at 475° C. Several lower aluminum patterns of 10 kÅ thickness were plated with 10 kÅ of Si02 at 475° C. Visual inspection of the wafers immediately after deposition revealed normal, bubble-free glass with

no cracks visible. The fact that the glass was virtually crack free and pinhole free was shown by etching a wafer in an aluminum etchant for 1 minute at 60° C. (Normal time needed to remove aluminum in this etchant is about 45 seconds.) There was no evidence of aluminum etching anywhere on the wafer. An etch rate taken on another wafer was the same as for the case of glass deposited at 400° C, indicating that the structure of the glass was unchanged.

Still another wafer was placed in a 475° C furnace for 15 minutes. Inspection after this heat treatment showed the glass was severely cracked, with the cracks emanating from the aluminum metalization.

It appears that an increase in deposition temperature is not a sufficient cure for the problem of cracking of vapor plated glass during exposure to temperatures above 475° C.

2.5 ETCH RATE AS FUNCTION OF PLATING RATE

The etch rate of plated oxide in buffered HF has been used as a check of the oxide structure and quality. Variation in the plating conditions has been found to have little effect on etch rate, even though the plating rate may change from 0 to 8kÅ/min. Another indication that glass structure is independent of the plating conditions was obtained by varying the substrate temperature and determining the resulting etch rates. Table 2 gives the results of that test.

TABLE 2

TEST RESULTS INDICATING INDEPENDENCE OF GLASS STRUCTURE RELATIVE TO PLATING CONDITIONS

Plating Temperature (°C)	Plating Rate (kÅ/min)	Etch Rate* in Buffered HF (Å/sec)
350	4.0	165
375	5.0	170
400	6.0	160
425	6.6	165
450	7.5	165
475	7.5	165
500	7.5	170

* The accuracy of this measurement is within ± 10 Å/sec.

2.6 PREVENTION OF ELECTROLYTIC ATTACK OF ALUMINUM

One of the predominant failure mechanisms for unsealed units in humid ambients is the electrolytic corrosion of the aluminum metalization. One would expect a layer of glass to provide a degree of protection against electrolytic corrosion. Several tests on a variety of structures indicated this is the case. However, on the structures being used on this study program, it must be pointed out that the aluminum bonding pads are not protected, and therefore the complete protection against corrosion is not obtained. An improvement is made because the spacing between bonding pads is large compared to the separations between metal interconnects within the circuit.

As a demonstration of the protection provided by a glass coating, three types of units were tested:

1. Unglassed (control),
2. Glassed in wafer form (as the units for this program will be),
3. Glassed after assembly (although this is considered impractical as a general technique for reasons discussed in Section 4).

The test consisted of covering each unit with water, and applying voltage between package leads 7 and 10 (see subsection 3.5) sufficient to cause 10 μA to flow. The units were then dried and electrical continuity was checked between package leads 7 and 10.

TYPE OF UNIT	PERIOD OF VOLTAGE APPLICATION	ELECTRICAL CONTINUITY
Unglassed	5 sec	No
Glassed in Wafer Form	5 sec	Yes
	10 sec	Yes
	15 sec	No
Glassed After Assembly	5 sec	Yes
	20 sec	Yes

The results of the above described test indicate that glass does provide additional protection for aluminum. However, without additional protection to avoid moisture condensation, glass encapsulation is not sufficient to prevent ultimate failure.

SECTION 3 - DESIGN STUDY

3.1 INTRODUCTION

The intent of the design study is to completely understand and document the mechanisms leading to bipolar device instability to evolve a glassing process and other design considerations which would most effectively improve microcircuit stability by the addition of a glass passivating and encapsulating layer. While much has been done to demonstrate the existence of mechanisms by which charge can be moved above a p-n junction, there has been little direct application of this knowledge to present state-of-the-art microcircuits.

Measurements made on the vehicle initially recommended for this program prove that the device stability and general construction do not permit the demonstration of any instability which might be reduced with glassing. This section describes the results of early tests on the initial vehicle. An improved approach is described for the study of surface charge accumulation through direct inversion methods. These methods more clearly define the fundamental mechanisms and the vehicle characteristics which would more likely demonstrate instability. The latter portion

of this section describes the new vehicle which is basically a high resistivity analog microcircuit indentical to a current product being manufactured by Philco-Ford. Tests have shown that glassed microcircuits are more stable in the presence of ambient contamination than are unglassed devices.

3.2 STUDIES PERFORMED ON INITIAL VEHICLE

3.2.1 Description of Vehicle

The initial test vehicle was previously described in the First Quarterly Progress Report. The vehicles were constructed from wafers which already had been diffused according to the fabrication process of a currently-marketed, standard dual three-input RTL gate. Figure 1 is a photograph of such a chip after glassing. The metalization pattern is unique to this program in that it makes available several individual components used in the circuit to permit more sensitive electrical evaluation than possible from circuit parameters. This model was to be used for assessing the stability of typical devices used in bipolar microcircuits.

Devices were prepared both with and without an additional layer of vapor plated glass. The unglassed test vehicles were made to study the inherent stability of standard-processed integrated circuits. The fabricated chips were assembled in TO-5 packages and then subjected to various tests to determine their stability.

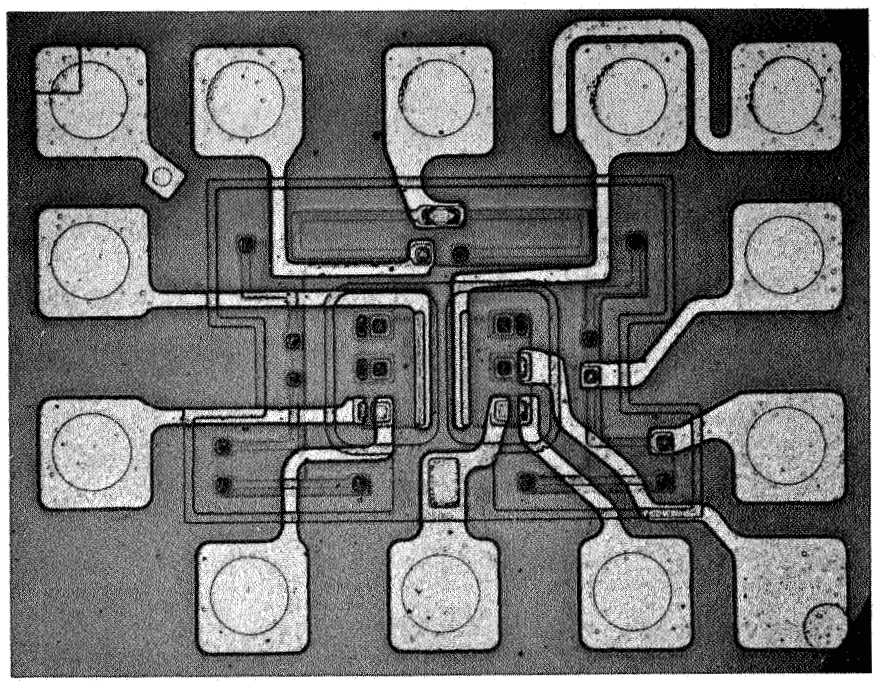

Figure 1. Dual 3-input RTL gate after glassing.

3.2.2 Tests and Results

The mechanisms which affect microcircuit stability and which will be improved by the addition of a glass layer were discussed in detail in the First Quarterly Progress Report. The principal mechanism is the fringing field which exists about a back-biased junction and may accumulate charge on the oxide surface of the device. This accumulated surface charge could then induce inversion layers in the underlying silicon[1-5].

The initial measurements made on the test vehicles were designed to reveal the effects of these fringing fields on the stability of bipolar devices used in microcircuits. A secondary objective was the preliminary assessment of the extent to which glass improves device tolerance to the effects of fringing fields. Because specific mechanisms were being studied, it was expected that a test could be devised to which every device would respond. Lengthy tests (1000 hours or more) or those resulting in changes in only a small percentage of devices were considered undesirable for these studies.

Conditions were chosen which accelerate device degradation caused by fringing field effects. These stability tests consisted primarily of subjecting devices to reverse biased conditions at elevated temperatures[1-5], such as 170° C, or to high humidity ambients with bias applied. Since one of the obvious

improvements obtained by glassing a microcircuit is redundant hermeticity, most tests were run on unsealed units, simulating leaky packages. Although very few TO-5 type packages assembled into systems can be considered "leakers", a small percentage of other types of packages have been found to be nonhermetic.

The device parameters most sensitive to degradation are I_{CEO}, I_{CBO}, BV_{CBO}, and low current beta (I_C = 30 to 50 μA).

Despite a wide variety of selected test conditions, ten of which were specified in the First Quarterly Progress Report, no significant permanent change in device parameters could be obtained. Several dozen devices were subjected to tests of this type during the first and second quarterly periods without significant degradation. It became apparent that even the individual components of these microcircuits were relatively insensitive to inversion layers formed by junction fringing fields.

In addition to the data from the 170° C tests and the 80° C, 70% relative humidity tests, results of tests conducted under another program[6] became available for analysis during the second quarterly period. These tests were conducted on glassed and unglassed microcircuit components made with the same manufacturing processes being used in the construction of the above vehicles. However, these units were face-down bonded to a printed circuit board, and encapsulated only in epoxy. The tests consisted of:

A. 43 units, 2000 hrs., 200° C storage with no applied bias

B. 38 units, 2000 hrs., 125° C with 4.5 reverse bias on emitter-base and collector-base junctions.

These tests revealed no significant degradation in either glassed or unglassed devices.

In an attempt to reduce the inherent stability of bipolar devices, samples were made from which the phosphorus glass, formed during emitter diffusion, was removed before metalization, (It is well known that the phosphorus glass ties up mobile alkali ions, thereby imparting considerable stability.) The tests conducted were with emitter-base and collector-base reverse bias at 170° C for several hours. Although initial tests produced instability on the units from which the phosphorus glass had been removed, subsequent tests have failed to reproduce degradation. These later results indicated that even without phosphorus glass, typical bipolar devices demonstrate considerable stability under conditions which promote surface ion accumulation. Since bipolar devices are generally not produced without emitter phosphorus glass, we are planning no further tests with this type of artifical vehicle.

As a result of the data accumulated on these tests, we found it necessary to revise the model. Specifically, a new approach to measuring device stability was necessary. The revised models are discussed in subsequent sections of this report.

3.3 TESTS OF DLRECT INVERSION

3.3.1 Introduction

As results of the tests described in the preceding subsection became available, it became apparent that the bipolar devices commonly used in digital microcircuits are relatively insensitive to surface charge separation produced by junction fringing fields. To ascertain the amount of surface charge necessary to invert the silicon surfaces being studied, we used a tool provided by MOSFET technology. This tool is described in detail below.

To determine the surface fields necessary to separate charge, voltage was applied between conductors on the surface. There are two structures which allow direct quantitative detection of inversion layers and have proven to be very useful in the study of surface effects on device stability. It should be emphasized that the data obtained are directly applicable to bipolar microcircuits since, although we are now using a study structure which is not a transistor, only the metalization has been altered and the silicon surfaces being studied are still in fact the surfaces of double diffused microcircuits. This is in keeping with the philosophy presented in the First Quarterly Progress Report, i.e., correlation is desired for the surface studies reported in the literature on particular silicon surfaces to state-of-the-artbipolar microcircuits.

The study of these structures has proven very fruitful in contrast to the studies described in the preceding subsection. This subsection presents a detailed discussion of the theory, the tests, and test results. Unless otherwise specified, the devices used in the tests reported in this subsection were unglassed and unsealed.

3.3.2 Theory

The First Quarterly Progress Report presented a chart which could be used to determine the surface charge required to invert silicon surfaces as a function of their resistivity (ignoring Q_{ss}). A significant advance in the progress of this program was made when we observed that surface charge could be applied directly by using an MOS capacitor structure. Consider a parallel plate capacitor as sketched in Figure 2 below. The voltage applied can easily be related

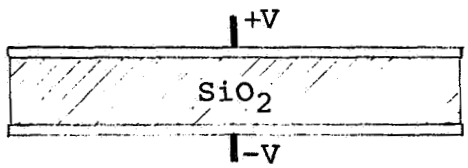

Figure 2. Basic SiO_2 capacitor structure.

to the surface charge density using the familiar formulas:

$$C\ [fd] = \frac{Q\ [coul]}{V\ [volt]} \tag{1}$$

$$C\ [fd] = \frac{8.85 \times 10^{-10} KA\ [cm^2]}{d\ [cm]} \tag{2}$$

$$\frac{Q\ [electronic\ charges]}{A\ [cm^2]} = \frac{1}{V\ [volts]} \cdot \frac{8.85 \times 10^{-10}}{d\ [cm]\ 1.6 \times 10^{-19} \left[\frac{coul.}{electric\ charge}\right]} \tag{3}$$

See Figure 3 for plots of surface charge for two typical oxide thicknesses. Since typical oxide thicknesses over the p-type base and n-type collector regions are 6000 Å and 9000 Å, respectively, we obtain for *p* type:

$$\frac{Q/A}{V} = 3.7 \times 10^{10} \quad \frac{\text{electronic charges}}{\text{cm}^2} \quad /\text{volt},$$

and for *n* type:

$$\frac{Q/A}{V} = 2.5 \times 10^{10} \quad \frac{\text{electronic charges}}{\text{cm}^2} \quad /\text{volt}.$$

These constants may be used to determine the voltage necessary on the plate of an MOS capacitor to invert the silicon "plate". Figure 4 is such a plot.

The next step in the utilization of this concept consisted of fabricating the appropriate capacitors. In principle, this presented no problem, since on integrated circuits the emitter metalization (or expanded contact) always crosses the oxide over the base region, and the base metalization often crosses the oxide over the collector region. By separating the emitter metal conductor from its contact to silicon, a plate is formed allowing inversion of part of the base surface. Note that to invert a p-type base, positive bias would be applied to the plate so as to attract electrons to the surface of the p-type silicon. This would result in conduction between the n-type collector and emitter.

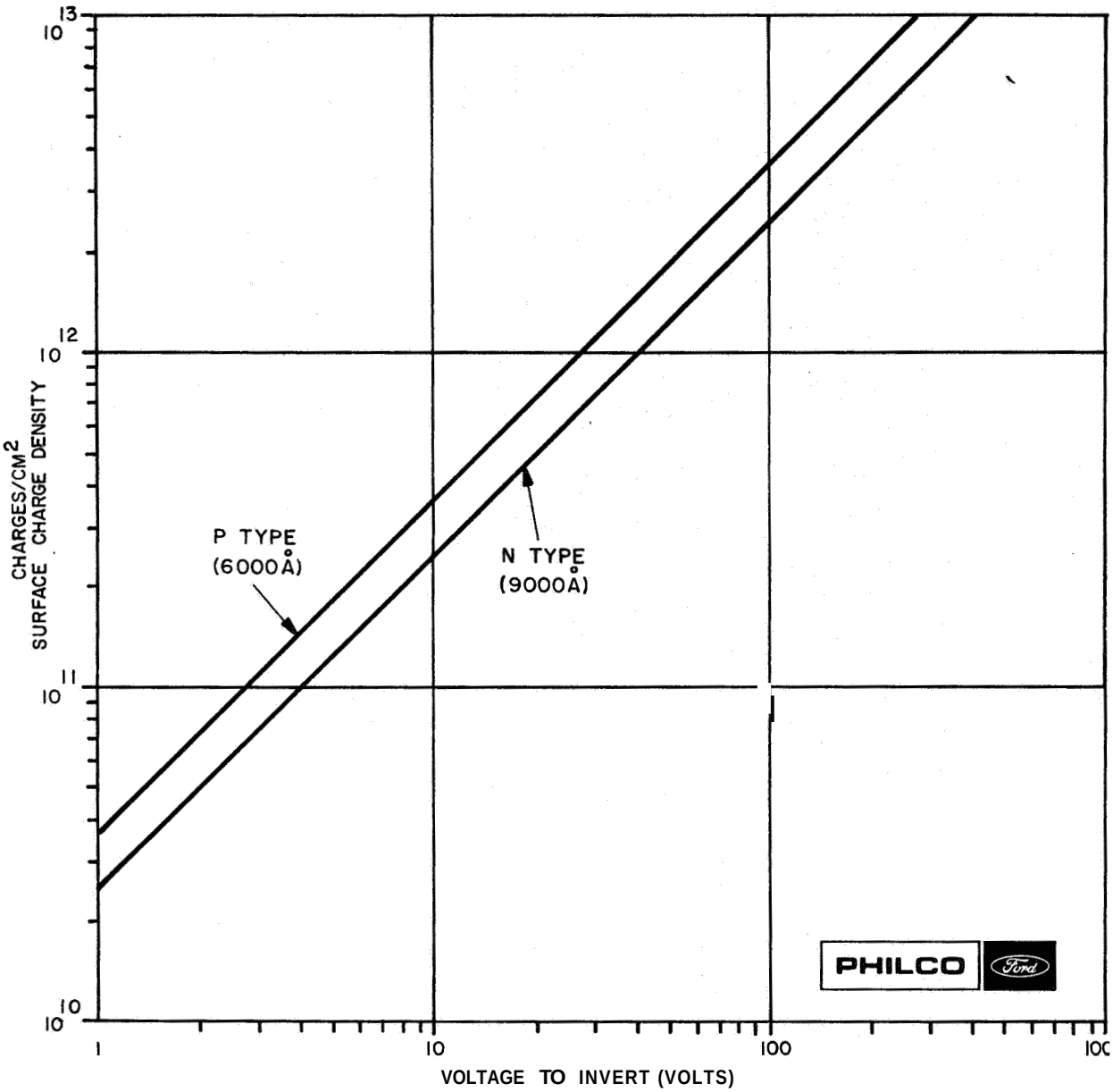

Figure 3. Surface charge as related to the equivalent voltage required for inversion.

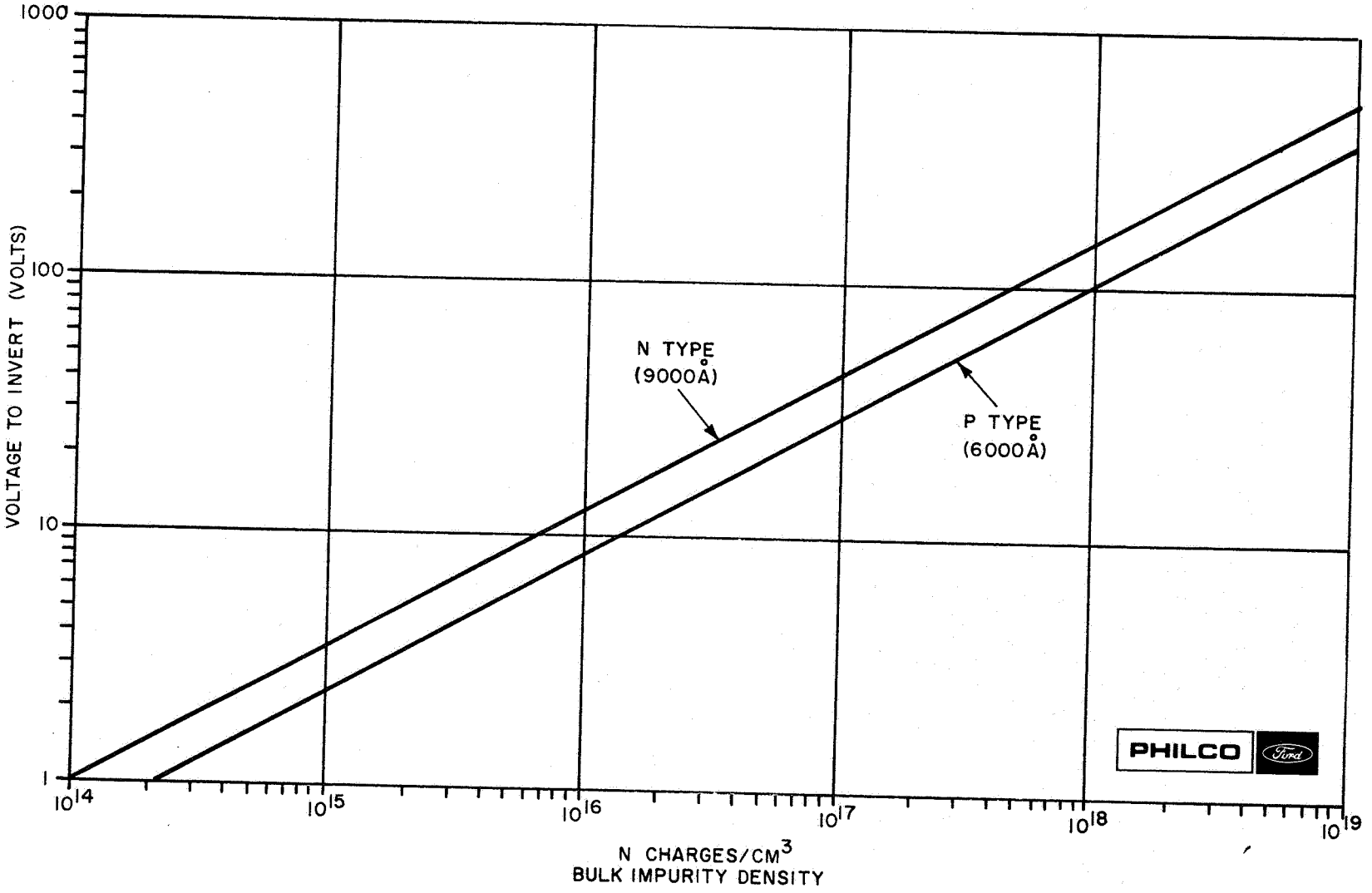

Figure 4 Voltage required to invert a given bulk impurity density.

A tool thus exists which immediately and predictably allows quantitative assessment of the amount of surface charge necessary to invert the base surface. Alternatively, by varying the voltage applied to this structure, the effect of surface charge can be correlated to transistor device parameters, the most sensitive of which are expected to be low current beta, BV_{CBO}, I_{CBO}, I_{EBO} and I_{CEO}. For example, when the base surface has been completely inverted, I_{CEO} will increase linearly with increasing voltage on the "gate" or metal over the base region.

The preceding model is useful in assessing the influence of a given amount of surface charge on underlying silicon, but does not permit assessment of the manner in which surface charge may accumulate. A second structure is used to enhance the surface charge separation due to surface fields. Since one of the mechanisms by which an additional layer of glass over a microcircuit will improve device stability is the prevention of surface ion motion in the presence of surface contamination, it is important that this mechanism be studied.

The "classical" degradation mechanism is the existence of surface fringing fields from back biased junctions, indicated in Figure 5.

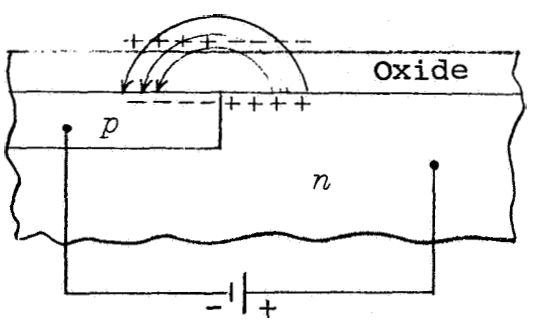

Figure 5. Sketch illustrating surface fringing fields associated with a back biased p-n junction.

The lateral surface field results in charge accumulation which attracts charge to the silicon surface, producing degradation of device performance. Since the tests on back biased junctions, as described in paragraph 3.2.2, failed to produce enough instability on short duration tests to be useful as a study tool, lateral surface fields were set up between conductors on the oxide surface as indicated in Figure 6. The fields set up with this structure could

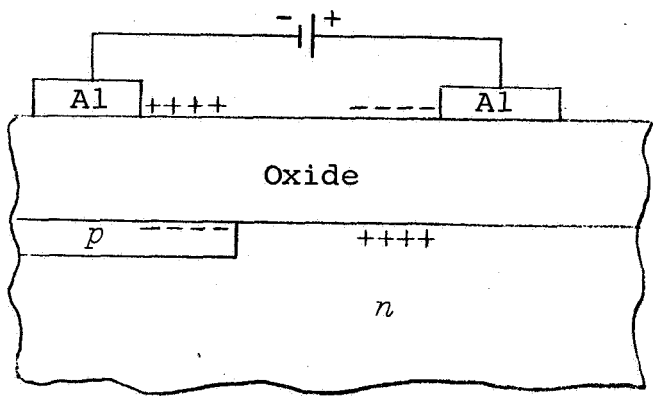

Figure 6. Sketch illustrating lateral surface fields setup.

be much higher than obtained with fringing fields (limited by diode breakdown), thus resulting in acceleration of charge accumulation. Note in this case that to invert a p region, negative bias is applied to the plate in contrast to positive bias for the capacitively induced charge. This condition of surface fields set up between metal conductors is a situation present on all microcircuits.

A quantitative theoretical treatment of the structure sketched in Figure 6, is impractical because of the variation in surface conditions. The amount of charge accumulated per unit field impressed

will be a function of surface conductivity, oxide contamination, time, temperature, etc. The usefulness of the structure depends on the ability to obtain high lateral surface fields. This in turn allows rapid accumulation of surface charge. Since the accumulation of surface charge depends on the surface condition and the ambient to which it is exposed, devices whose surface (that on which the metal interconnects are formed) is protected by an additional glass layer will respond differently than devices with unprotected surfaces.

This structure has several disadvantages which should not be minimized. Referring to Figure 5 it will be noted that in addition to performing the desired function of attracting surface charge, a surface plate can itself induce (through a capacitive effect) charge to the surface of the silicon. With the polarity shown, these will be accumulation layers rather than inversion layers, but the extent to which the accumulation layer compensates the inversion is difficult to determine. Obviously, care must be used in placing the surface plates on the device so as to minimize capacitive inversion.

Another, even less well understood, undesirable mechanism is the collection of surface charge by a surface plate. Even if the plate does not collect surface ions it may neutralize them. If the charge is attracted too strongly, it will travel beneath, or on top of, the surface plate and no longer be effective in causing inversion.

A parasitic mechanism common to both capacitive and surface-field-induced inversion is the possibility of the altered effective doping concentration changing the leakage of the back biased junction (for I_{CEO}, the collector-base) before true inversion of the base surface occurs. The effect of this mechanism can be eliminated by an experimental technique, as described in paragraph 3.3.3. The point is that for high voltages on the surface, an increase in I_{CEO} may not be an indication of base inversion.

Despite its disadvantages, the surface plate structure has proven to be useful in the study of surface-charge-induced inversion. The presence of these unknowns simply complicates the understanding and interpretation of experimental results. Generally speaking, stray capacitive effects are eliminated by shorting all metal leads together. Since surface charge motion is relatively slow in dry ambients, the surface-charge-induced effects will remain. Application of moisture will drastically alter the surface effects but has little influence on capacitive effects.

3.3.3 Capacitive Inversion

Several devices were constructed to facilitate the study of direct inversion. A field was applied between the Si material and a metal plate on the SiO_2. The devices consisted of standard, metalized integrated circuits upon which the metalization was mechanically isolated from the underlying silicon in predetermined locations.

The isolated metalization extended across the region being investigated over the adjacent oppositely-doped regions. Figure 7 is a photomicrograph of one of the initial structures used to study inversion. Inversion of a specific region could be created by applying a voltage of the correct polarity (+ for *p*, - for *n*) to the isolated metal with respect to the underlying silicon. The degree of inversion can be directly related to the conductivity between the two regions separated by the region being inverted, much in the manner as an MOS transistor. The conductivity was determined by measuring the current at a constant applied voltage. On a bipolar transistor whose base is being inverted, this parameter is essentially I_{CEO}.

Tests were initiated to characterize the surface charge density necessary to cause inversion of the various resistivity regions present in a microcircuit. The initial test consisted of modifying an integrated circuit transistor so that metalization over the base was isolated as shown in Figure 7. In MOS terminology the source, gate, and drain were the emitter, isolated metal, and collector, re-repectively. A voltage of up to 300 V was applied between the isolated metal and the base region. The parameters observed were the same as those monitored in the tests described in subsection 3.2, i.e., I_{CEO}, low current beta, and breakdown voltages. Although shifts in other parameters could be detected, I_{CEO} was by far the most sensitive. This was somewhat surprising since published results had led us to expect low current beta to be a strong function of surface conditions. On

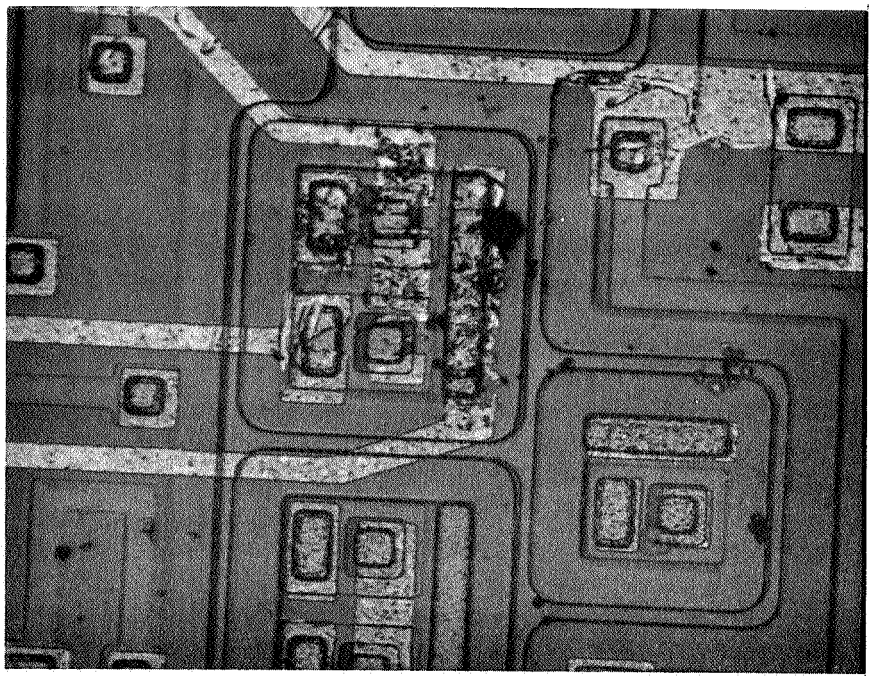

Figure 7. Modified metal pattern to study inversion of a base region.

the other hand, the base surface plate does not completely overlap the emitter-base or collector-base junction so its effect on beta might not be expected to be as pronounced as on I_{CEO}.

Direct capacitive inversion tests were made using structures having n-type epitaxial layers in the resistivity range from 0.2 R-cm to 6 Ω-cm, and p-type diffused base regions. The test results are summarized in Table 3.

TABLE 3

RESULTS OF DIRECT CAPACITIVE INVERSION TESTS

N-Type (Homogeneous)	Calculated Inversion Voltage	Measured Inversion Voltage
4 to 6 Ω-cm	-3 V	**-15 V**
0.5 Ω-cm	**-11** V	**-21** V
0.2 Ω-cm	-22 V	**-28 V**
P-Type (Diffused)		
120 Ω/□	+350 V	**+140 V**
240 Ω/□	+175 V	**+70 V**

Referring to the test results given in Table 3, note that to invert n-type material, a voltage higher than the calculated value must be applied, whereas to invert p-type material a voltage lower than the calculated value must be applied. There are two mechanisms

responsible for this situation. One is the negative accumulation layer at the $Si-SiO_2$ interface which regults from the positive charge (Q_{ss}) normally present in the SiO_2 layer. The other is that the segregation coefficients of boron and phosphorus in silicon and SiO_2 are such that oxidized n surfaces are phosphorus-rich and oxidized *p* surfaces are boron-poor. Note that n-type silicon in the resistivity range of 4 to 6 Ω-cm, the range frequently used in high voltage analog devices, is susceptible to inversion with the voltages used in these circuits.

Although the use of this structure is generally quite straightforward, the technique does have its limitations, the most important of which are described below.

To check the inversion test technique described above, a voltage of opposite polarity to that necessary for inversion was applied between the silicon and isolated metal on several units. Since this results in an accumulation layer rather than an inversion layer, one would not expect a channel current. As expected, no increase in monitor current was observed for surface plate voltages below 100 V. However, when the plate voltage exceeded 100 V, an increase in monitor current was observed. The following theory is advanced to explain the cause of this increase in current.

The monitor current is initially limited by the leakage current across the reverse biased p–n junction. An increase in current can result from two effects: 1) an inversion layer shunting the two junctions, or 2) an increase in the current through the reverse biased junction. Since no inversion layer can be formed with the polarity applied, the junction leakage current must have increased.

The current through a reverse biased junction is determined by the equation[7]:

$$I_r = - \frac{qAD_p P_n}{L_p} + \frac{qAD_n N_p}{L_n} \qquad (4)$$

where P_n and N_p are the assumed minority carrier concentrations in the n and p regions, respectively. Assume we are studying an n region, electrons in the p region will be attracted to the surface. This results in an increase in the minority carrier concentration, N_p, at the p surface of the silicon. Therefore, from the preceding equation, I_r will increase.

An experiment was performed to test the preceding theory. A device was constructed that had a field plate running over one p–n junction only, (See Figure 8.) Since an increase in minority carrier concentration only affects a reverse biased junction, applying a field

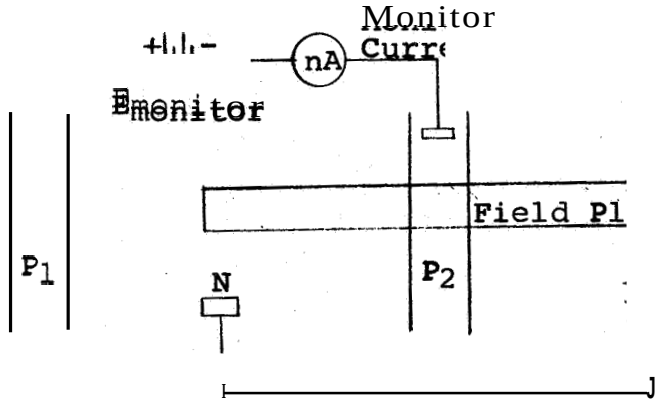

Figure 8. Test structure to determine influence of surface charge on junction leakage current.

over this junction should result in an increase in monitor current. Applying a field over a forward biased junction should not increase the monitor current. If the monitor voltage is positive, P_2N will be reverse biased and will be affected by the field; however, if the monitor voltage is negative, P_2N will be reverse biased and not affected by the field.

The experiment demonstrated that the reverse biased junction leakage was affected by the applied field. As a result of this test, it has been suggested that the reverse biased junction current be monitored between *p* and *n* in addition to the p-region to p-region monitor current. The current due to inversion of the *n* region would then be the difference between the two currents.

3.3.4 Surface-Field-Induced Inversion

In addition to the capacitive technique for obtaining surface charges, surface charge accumulation may occur when a field is set up an the surface of the planar oxide. Such a field can be created by applying a voltage between two isolated metalizations on the oxide surface. Any positive mobile ions should be attracted to the negative surface plate, and negative mobile charge should be attracted to the positive surface plate. The resulting accumulation of charge on the oxide surface can influence the underlying silicon, in some cases, creating inversion layers.

Devices were constructed, in much the same manner as described in paragraph *3.3.3*, from standard integrated circuits and the initial vehicle. On these devices, two metal conductors were mechanically separated to electrically isolate them from the silicon. These conductors were chosen to be nearly parallel, and one metal conductor extended across the three adjacent regions covered by the capacitor surface plate of paragraph *3.3.3*. The degree of inversion could therefore be observed by the same method as for capacitive inversion.

As in the structures described in paragraph 3.3.3, a p-type region will tend to invert when positive charge is on the oxide surface over it, since this positive charge induces a negative charge in the surface of the *p* region. To attract positive charge to the surface plate crossing the appropriate three regions, that surface plate is made negative with respect to the other surface plate. Note the negative polarity applied to the conductor in this case, whereas capacitive inversion requires positive voltage on the plate over a *p* region to induce inversion.

Devices were tested both with and without a condition that would increase ionic mobility, i.e., at a high temperature and with a moist ambient, and inversion layers were actually formed. Further, the inversion layer remained after the applied voltage was removed and the surface plates shorted to each other. This retained inversion could be removed by applying humid air to the surface or heating the device to about 150° C with no applied voltage. Since the inversion layer did

not disappear when the surface plates were shorted, the inversion layer cannot be attributed to capacitive effects as described in paragraph 3.3.3. The disappearance of the inversion when the conductivity of the surface oxide was increased supports the conclusion that surface charge accumulations were present.

An example of the type of tests conducted is shown in Table 4.

TABLE 4

SURFACE INVERSION TEST

(0.5 Ω-cm N-TYPE)

TEST STEP	*P-N-P* MONITER CURRENT at 1.5 V	CONDITIONS
Starting	1 *n*A	- - -
1	3800 *n*A	240 V applied for 10 min at 150° C, cooled to 250° C with bias, then bias removed.
2	1500 *n*A	75 minutes later at room temperature
3	1 *n*A	After blowing moist air on the surface of the chip

As a variation of the above test, the vehicle shown in Figure 9 was fabricated, also of 0.5 R-cm n-type material. The total initial p-n-p monitor current was measured and, in addition, the reverse biased p-n junction current was measured. The currents were approximately equal. A dc voltage of 240 V (any voltage over 50 V is sufficient) was applied between the two surface plates. The device was heated to approximately 150° C for 5 minutes to increase the mobility of the surface ions and was then cooled with the voltage still applied. After the device returned to room temperature, the surface voltage was removed, and both surface plates were shorted to the n region to discharge any capacitively formed inversion layers. The *p-n-p* monitor and junction leakage currents were again measured. The monitor current had increased by a factor of 300, while the junction leakage current was 40 times the initial value. Although both surface plates remained shorted for several minutes, very little change in the monitor current was observed. The monitor current could be returned to the initial value by blowing moist air onto the surface of the device.

The separation of metal conductors is difficult to achieve as it must be done mechanically. The results are not as clean as one would like, and this can be seen in the photographs in Figures 7 and 9, Further, the test data obtained from different devices subjected to indentical tests sometimes varied. This experimental variation could

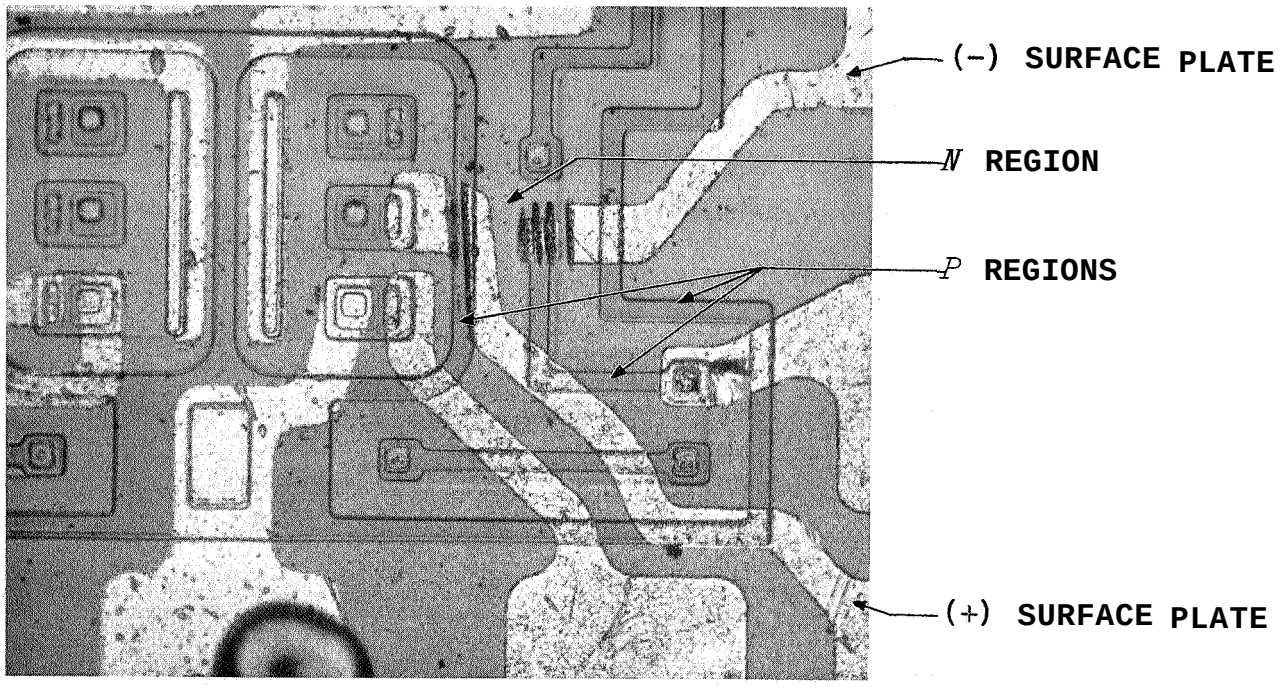

Figure 9. Initial structure as modified to study inversion of the silicon surface.

often be attributed to the variation in the geometry of the metalization from device to device. Therefore, we concluded that the initial test vehicle used for the evaluation phase of this program could profit from a redesign to include the structures described above.

3.4 DIRECT INVERSION STUDY VEHICLE

As the results of the studies on the two test structures were obtained (capacitive and surface inversion), it became obvious that such structures were capable of providing useful stability data. Available bipolar devices were still difficult to use in making rapid stability tests; it was necessary to redesign the test vehicle to include the two types of structures.

The revised vehicle retains standard diffusions and brings out electrical connections to standard bipolar devices, in addition to the improved stability sensing structures. The original intent of relating stability of the $Si-SiO_2$ interface to actual bipolar devices is thus still retained. In addition to the increase in sensitivity obtained from the inclusion of the new structures, a standard wafer utilizing a higher resistivity epitaxial layer was chosen to further increase the sensitivity. The wafers being used are the same as used to fabricate PA7709 circuits and are obtained from the production lines prior to metalization. Although wafers to be used will have transistors with BV_{CEO} values lower than the PA7709

specifications, we do not expect this parameter to influence the tests to be made.

A photomicrograph of a glassed chip ready for assembly is shown in Figure 10b. Each pad on the device is numbered corresponding to the flat pack lead to which it will be connected. The pad connections are listed below:

Device Pad and Flat Pack Lead No.	Connection To
1	Collector of test transistor.
2	Base of test transistor.
3	Surface plate to invert base of test transistor by capacitive (MOS) effect. Also to be used for inversion of base by accumulated surface charge.
4	Resistor for observation of n-region inversion.
5	Surface plate to invert underlying n region by capacitive (MOS) effect. Also used for *p* and n inversion by accumulated surface charge.
6	Isolated "bucket" n region.
7	Base of control transistor.
8	Emitter of control transistor.
9	Isolation.
10	Collector of control transistor.
11	Field plate (on those units having field plates).

12	Surface plate for inversion of isolation by capacitive (MOS) effect. Also used for n-region inversion by accumulated surface charge.
13	No connection,
14	Emitter of test transistor.

A photomicrograph of the chip before glassing is shown in Figure 10a. Note the absence of the circular contact cuts which are visible in Figure 10b. The addition of a field plate, a metal pattern completely covering the entire active region of the microcircuit, is shown in Figure 10c.

3.5 STUDIES PERFORMED ON REVISED VEHICLES

3.5.1 Capacitive Inversion

Tests were conducted on the new test vehicle to determine the voltage necessary to cause direct inversion. With capacitive inversion, no difference would be expected between glassed and unglassed chips since the charge is not being accumulated on the oxide surface but on the metal plate at the oxide surface. As expected, no differences were observed between glassed and unglassed units. The results for both types are shown below.

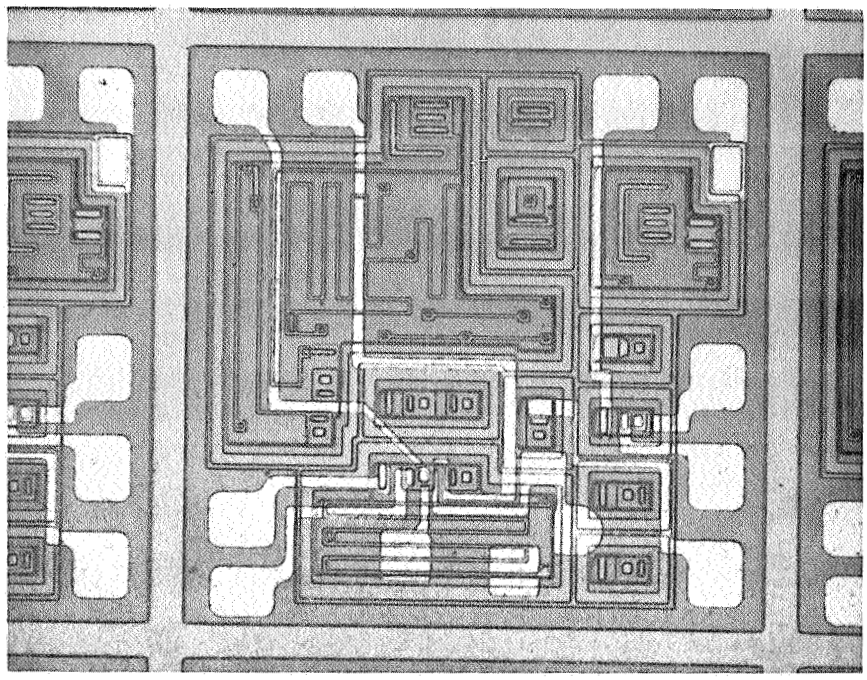

Figure 10a. Revised test device and metal pattern, before glassing.

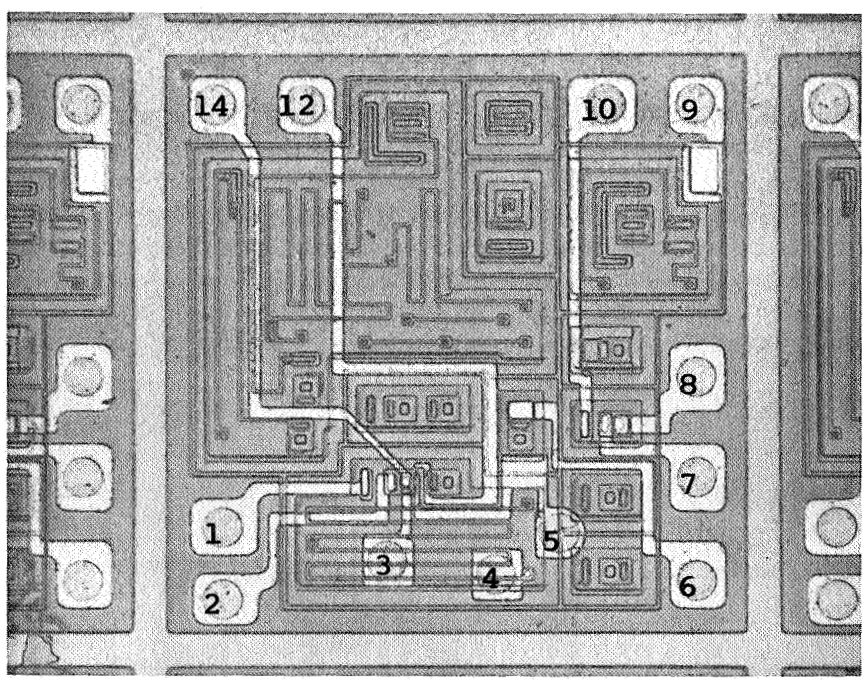

Figure 10b. Revised test device, after glassing and etching of contact cuts.

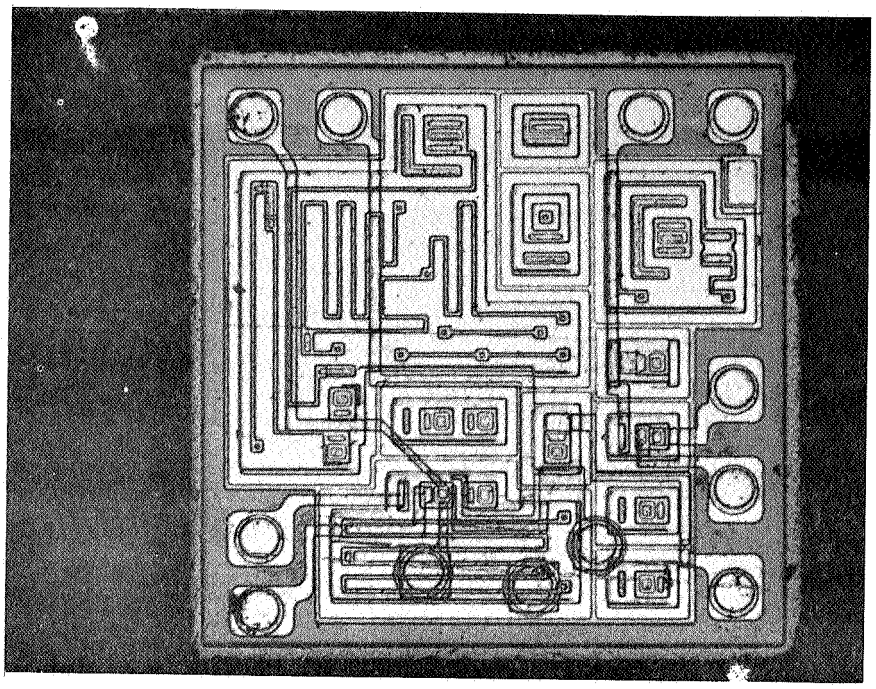

Figure 10c. Revised test device, showing addition of "field plate".

Type Region	Voltage Required to Invert	Charges/cm^{2*}
N (4 to 6 Ω-cm)	−22 V	6×10^{11}
P (diffused, 110 Ω-cm/□)	+60 V	2.2×10^{12}

* Taken from Figure 3.

The voltage shown above as required to invert 4 to 6 Ω-cm *n*-type silicon is higher than the voltage in paragraph 3.3.3 because of a change in measuring technique. Using the technique described in paragraph 3.3.3, inversion was considered to occur at that voltage at which the monitor current began to change. In order to make the measurement more reproducible, the inversion voltage was redefined as that voltage which causes an order of magnitude increase in monitor current.

There is a further difference in the voltage required to invert the *p* region because different diffusion schedules were used to obtain the sheet resistivities, apparently resulting in some difference in surface concentration. A deeper base-collector junction will have a lower surface concentration for a given base sheet resistivity.

The effect which direct inversion of the base has on low current beta and breakdown voltages was also studied on this vehicle; these parameters were found to be much less sensitive to inversion than is I_{CEO}.

3.5.2 Surface-Field-Induced Inversion

After some of the revised vehicles were fabricated, tests were performed to characterize the effectiveness of the surface field applied via the surface plates in creating surface charge accumulations on the surface of the oxide on unglassed devices (see paragraph 3.3.4). Although sufficient charge accumulations could readily be obtained to produce inversion, many of the test results are not well understood. As discussed in paragraph 3.3.2, the action of the field between the surface plates is not exactly indentical to junction fringing fields. Specifically, the field applied via the surface terminates on conductors, whereas fringing fields do not. However, the structure is identical to the case of metal conductors on a microcircuit and therefore perhaps worthy of study.

It must be stressed that the surface field structure described above is most likely to be useful in the study of long term degradation, unlike the MOS capacitor structure which quantitatively produces surface charge instantaneouly. The capacitor structure is only a measuring tool however, since inversion layers produced in this manner occur immediately, and devices having such inversion layers would never pass initial testing and so are not a reliability problem. Surface charge accumulation resulting from charge separation in a surface field is dependent on time (and other factors): therefore,

the results such as have been obtained by a test of a 'few minutes duration may be misleading.

The first tests conducted were similar to those described in paragraph 3.4.4. As reported in paragraph 3.4.4 inversion occurred in two devices that were subjected to 150°C with 270 V on the surface plates for 15 minutes. To further characterize the vehicle, test conditions were varied. Ten devices tested at 150° C but with only 200 V on the surface plate for 30 minutes also inverted. However, six devices subjected to 150°C with 180 V for 2 hours were not inverted at the conclusion of the 2 hours. Three devices submitted to 90° C with 270 V on the surface plates for 15 minutes did not invert. These results are consistent with those reported in paragraph 3.4.4, except for those from the 2 hour test which are not understood.

Measurements were taken after the devices cooled to room temperature and the surface plate voltage removed. The inversion described is retained after the applied voltage was removed and the surface plates shorted. Applying either humid air or heat to any of the above devices removed all the retained inversion.

In an attempt to promote surface charge accumulation, devices were subjected to a test chamber at 90°C with poorly controlled moist ambient for 72 hours with 90 V across the surface plates. Unfortunately, water collected on many of the devices such that the aluminum metalization was removed by electrolysis. This test will be repeated with better control of the humidity to avoid condensation.

At this point, with some confidence that the vehicle was adequate to sense surface inversion, testing of glassed devices was begun to assess the effectiveness of glass in preventing charge accumulation on the surface of the thermal oxide. While many of the tests produced the expected results, the behavior of some devices under test is not now understood. For example, in the above 150° C, 200 V, 30 minute test, glassed devices did not invert. This was as expected. However, after two hours at 150° C and 180 V, glassed devices were inverted: whereas, as pointed out above, the unglassed devices were not. To further complicate the model, when inversion was induced on glassed units, the inversion could not readily be made to disappear by blowing humid air on the surface.

At this point we changed the type of testing. We discovered that adding humid air to the surface of the chip was just as effective in increasing the surface charge mobility as was raising the temperature of the units. In addition, testing at room temperature avoids the possibility of charge movement within the oxide, a potential degradation mechanism which glassing will not alter.

Subjecting both glassed and unglassed devices to this sort of testing demonstrates that the glassed devices generally show less sensitivity to the humid ambient than do unglassed devices. For example, one of the simplest tests is to have the operator blow on an exposed unit while a voltage is applied to the surface plates. A typical voltage on the surface plates is 50 V. An unglassed unit

will invert immediately; a glassed unit typically is unaffected. This sort of test was demonstrated to **NASA** personnel during their visit to the Philco-Ford facilities at Blue Bell, Pennsylvania on March 22, 1967.

Disadvantages of blowing on the units are: 1) the uncontrolled conditions and, 2) the possibility of moisture condensation on the chip surface. **A** bubbler at room temperature with N_2 flowing through as a means of obtaining humid, but not supersaturated, ambients is now being used.

As a final example of the type of tests being conducted, the data in Table 5 are typical. In general, the test results recorded in Table 5 follow the model proposed and therefore indicate that the test structure may be useful in the study of surface charge accumulations. However, in specific instances the model is inadequately characterized, accentuating the need for further investigation.

TABLE 5

DATA FROM TYPICAL TESTS BEING CONDUCTED
TO STUDY INVERSION LAYERS FORMED BY SURFACE CHARGE

TEST CONDITION	PNP CURRENT -- μA at 5 V									REMARKS
	UNGLASSED				GLASSED					
	1	2	3	4	5	6	7	8	9	
1. Initial.	0	0	0	c	C	0	0	0		These data indicate the n region is not inverted initially. (This is as one would expect.)
2. Apply 50 V to surface field plates (polarity as discussed in the text).	3	0	3	E	C	0	0	0	0	As expected, no Inversion exists (except for the slight inversion of Units 1 and 3).
3. Apply humid air.	20	14	21	1	5	0	0	0	0	One would expect the unglassed devices to invert (because they are sensitive to surface humidity), and the glassed devices not to invert. Except for Unit 5, the glassed devices behaved as expected.
4. Turn off humid air and blow on dry air.	20	14	21	1	5	0	0	0		One would expect these data because once the surface charge has been allowed to accumulate, returning to dry ambient only "locks" in the charge.
5. Turn off the applied voltage and short the surface field plates.	0	0	0	a	c	0	0	0	0	Once the surface charge has been allowed to accumulate and is "locked" in by drying the surface, one would expect the charge to remain after removal of voltage. These results are not typical for this test condition. Perhaps the surface was not sufficiently dry.
6. Apply humid air..	0	0	0	0	C	0	0	0	0	Applying humid air allows the surface charge to redistribute, and the units would be expected to return to the initial state. Of course, in this particular test, no inversion remained from the previous step.
It was demonstrated in several types of tests that surface-field-induced charge accumulations can be additive to capacitor type surface charge. That is, if a voltage applied between a surface plate and silicon is sufficient to create a small inversion layer in the silicon, this inversion can be made more pronounced by biasing the surface plate properly with respect to other surface plates. Therefore, the testing of the units was continued as follows.										
7. Remove humid air and apply dry air.	0	0	0	0	0	0	0	0	0	No inversion exists initially.
8. Apply 50 V to surface field plates.	3	0	6	0	0	0	0	0	0	Same remarks as for Test Condition 2.
9. Apply 50 V between silicon and surface field plate (capacitive inversion).	32	15	38	20	32	25	30	23	24	Significant inversion exists on both glassed and unglassed units. This is capacitive inversion and no difference should be expected between the glassed and unglassed units.
10. Apply humid air.	112	110	120	100	63	75	85	77	76	As expected, more inversion is created in the unglassed units due to surface charge reparation. Inversion is also enhanced on glassed units, which was not expected. Note, however, that less increase occurred on the glassed units.
11. Remove humid air and apply dry air.	112	110	120	100	63	75	85	77	76	The surface charge has accumulated and is "locked" in.
12. Remove capacitor voltage.	80	75	80	78	20	48	55	50	56	The capacitive inversion has been removed (subtracting the pnp current of this test condition from that of 10 typically gives that of 9). Note the difference though between the pnp currants of Test Condition 8 and 12. This is retained Inversion thought to be due to surface charge accumulation. Note that the glassed units have less surface charge accumulation than do unglassed units; actually it was expected that the glassed units wuld have none.
13. Remove voltage from surface field plates.	23	20	25	17	0	3	12	4	5	Since the surface charge accumulation is not free to redistribute (the surface is "dry"), such a large change vas not expected. (See remarks for Test Condition 5) Perhaps a mechanism other than surface charge accumulation exists. Note, however, that a much large amount of inversion remains on the unglassed units than on the glassed units.
14. Apply humid air.	0	0	0	0	0	0	0	0	0	The applied humidity allows tht surface charge to redistribute and, as expected, the devices returned to their initial, uninverted condition.

3.6 SUMMARY

Analyzing the results from the tests has been difficult. There are two ways to cause inversion of silicon: 1) by direct inversion, applying a voltage between a metal conductor on the surface of the oxide and the underlying silicon, or 2) by the accumulation of charge on the surface by applying a voltage between conductors on the surface of the oxide. Difficulties have been encountered, as stated in paragraph 3.3.2, in applying conditions to cause one type of inversion without, at the same time, producing the other type. The outstanding difference between the two means of causing inversion is the degree of dependency upon time. Experiments have generally shown that capacitive inversion is an instantaneous effect, with inversion occurring immediately upon the application of a voltage, and disappearing immediately upon removal of that voltage. Surface-charge-induced inversion occurs with a time delay, since the mobility of the ions on the oxide surface is much lower than the mobility of charge in silicon and metal. For this reason, accumulated surface charge is retained for a considerable period of time after the applied voltage is removed. We used these differences in behavior to determine whether inversion is capacitive or a result of the accumulation of charge on the surface of the oxide.

3.7 REFERENCES

1. M.M. Atalla, A.R. Bray, and R. Linder, "Stability of Thermally Oxidized Silicon Junctions in Wet Atmospheres," Proc. IEE (London), 106, Part B, 1130-1137 (1959).

2. E.D. Metz, "Silicon Transistor Failure Mechanisms Caused by Surface Charge Separation," pp. 163-172 in PHYSICS OF FAILURE IN ELECTRONICS, 2, Ed. by M.F. Goldberg and J. Vaccaro, Rome Air Development Center, Rome, New York, 1964

3. G.L. Schnable, E.S.Schlegel, and R.S. Keen, "Failure Mechanisms in Reverse-Biased Oxide Passivated Silicon Diodes," pp.108-121 in PHYSICS OF FAILURE IN ELECTRONICS, 3, Ed. by M.F. Goldberg and J. Vaccaro, Rome Air Development Center, Rome, N.Y., 1965.

4. W. Shockley, W.W. Hooper, H. J. Queisser, and W. Schroen, "Mobile Electric Charges in Insulating Oxides with Application to Oxide Covered Silicon p-n Junctions," Surface Science, 2, 277-287 (1964).

5. J.J. Licari and G.V. Browning, "Plastics for Packaging; Handle With Care", ELECTRONICS, April 17, 1967, pp. 101-108.

6. S. Wagner and W. Doelp, "Low Cost Integrated Circuit Techniques", Technical Report ECOM-01424-F, Final Report on Contract DA28-043 AMC-01424 (E), May 1967.

7. A.B. Phillips, Transistor Engineering, McGraw-Hill Book Company, Inc. New York, 1962, p. 107.

SECTION 4 - MANUFACTURING STUDY

4.1 REASONS FOR GLASS APPLICATION

In deciding when to apply a protective layer, such as SiO_2, during the manufacturing process, the reasons for applying such a coating should be considered. These may include any or all of the following:

1. To protect the relatively soft aluminum metal used for interconnections on both bipolar and MOS devices;
2. To increase the dielectric layer thickness, thus reducing the capacitive effect between metal interconnects and the substrate;
3. To provide an insulating layer for use in depositing multilevel interconnections;
4. To provide protection from ambient contamination.

4.1.1 Protection for the Aluminum

In most manufacturing processes the wafer is reduced to individual microcircuit chips through a process of scribing and breaking. This frequently results in considerable damage to the aluminum interconnections because of abrasion from particles of silicon generated during the operation. A protective layer, such as photoresist, has been shown to be helpful in reducing such damage. However, this organic must be removed before subsequent assembly. If a layer of

glass were utilized in this manner it need not be removed after further processing. However, contact holes must be etched in the layer to permit connections to the underlying bonding pads.

4.1.2 Increasing Dielectric Thickness

The discussion presented in the Appendix indicates the desirab Lity of a thick dielectric layer to reduce the capacitive effect between metal layers, and between the metal layers and the substrate. The maximum thickness of the thermally grown oxides used in processing the active device is determined by the required device geometry. Thus the ability to deposit an additional dielectric layer following completion of the normal processing steps is desirable for reducing parastic coupling.

4.1.3 Providing an Insulating Layer

Within the past two years there has been an increasing demand for the ability to make metal interconnects of sufficient complexity when more than one layer is required. The present bipolar integrated circuit technology has an inherent crossover capability in that a metal conductor can pass over a diffused resistor. It sometimes is required on bipolar devices and nearly always on MOS devices, that a high concentration, low resistance diffusion region be created specifically for crossover areas.

More complicated functions involving hundreds of components necessitate the addition of an insulating layer to completely cover

the first normal level of metal. Through-connections (vias) are achieved by etching a path in the dielectric and continuing with the next level of metalization.

4.1.4 Providins Protection from Ambient Contamination

As stated at the beginning of this section, a glass layer can provide some protection of aluminum from mechanical damage. It has also been shown that the aluminum metal is quite susceptible to electrolytic corrosion when exposed to moist ambient conditions. Thfs could occur in hermetically sealed enclosures which have failed and developed a leak as well as on chips packaged in a non-hermetic environment. Therefore, glass can provide desirable protection.

When considering the influence of ion migration on the surface of a microcircuit, it becomes desirable to place an additional dielectric layer over the complete microcircuit surface. This would inhibit the separation and migration of ions on the original oxide surface. Such charge separation can result from fringing fields as well as from lateral surface fields due to potential differences between metal conductors. Ion contamination would be further excluded from the substrate by the additional dielectric layer and would thus be less likely to cause a parameter change.

As stated in the Appendix, more complete freedom from ion migration can be achieved by the subsequent application of a phosphosilicate or a metal field plate. The phosphorus glass has

been shown to act as an effective getter for sodium and hydrogen ions. A metal plate would eliminate the possibility of lateral fields.

4.2 DETERMINING POINT OF GLASS APPLICATION

From an economic viewpoint, a greater number of circuits can be glassed in wafer form than in a partially or completely assembled form, simply because of size. Moreover, the glass layer applied in wafer form will still provide the redundant protection desired for hermetically sealed devices. It should be noted that applying the glass to the wafer would not preclude the deposition of an additional glass coating following assembly. Although the latter deposition method would more completely coat the entire structure, it would have the disadvantage of undesirable depositions of glass on the peripheral members of the package. In addition, the assembled chip has temperature limiations imposed by the gold-silicon eutectic (melting point 367° C) frequently present in microcircuit assemblies.

The following considerations should be noted regarding bonding to a microcircuit chip which has been covered with a layer of glass. If the bonding pad is to be exposed by etching through the glass layer, the opening should be made somewhat smaller than the pad termination to guarantee that the etchant will not reach the normally present oxides. Such a condition could lead to undercutting in the critical bonding pad area. Therefore, the area for bonding on a glassed unit will be less than that on an unglassed one.

In addition, although more work is required in this area, it appears that thermocompression bonding to the exposed bonding pad is sometimes more difficult than ultrasonic bonding of aluminum wire. This is most likely a result of the ultrasonic bonding breaking through any residual glass coating which may be present in the bonding area.

A possible solution for both of the preceding problems would be the formation of the bonding pad on the top surface of the deposited coatings. A through connection or via requires less area than a bonding pad; hence the connection from the bonding pad to the'underlying metal can be made without concern about the chip size. Such an approach, however, does imply additional processes since two levels of metalization must be present.

4.3 SUMMARY

With so many possible utilizations of an additional coating in the fabrication of silicon integrated circuits, it would be desirable to employ a glassing process which would be broadly applicable to the many purposes for which glass can be utilized. We therefore, recommend that depositing a SiO_2 layer by oxidation of silane is a proper selection and will permit the goals of this specific program to be achieved. We further recommend that the glass be deposited while the product is still in wafer form, before reduction to individual chips.

SECTION 5 - DEVICES FOR PERFORMANCE EVALUATION (TASK III)

5.1 DESCRIPTION

The devices for the performance evaluation will be the same devices as those described in subsection 3.4. These vehicles will be from PA7709 circuit wafers with special metalizations. Four groups of test vehicles are being prepared:

1. Unglassed, open
2. Unglassed, sealed
3. Glassed, open
4. Glassed, sealed.

A few devices incorporating field plates may also be assembled for testing. All of the above devices will be assembled into 14-lead flat packs. Aluminum whisker wires will be attached by ultrasonic bonding. The PA7709 circuits are normally assembled into TO-5 packages, but since it is desired to have available 13 leads on the test vehicle, flat packs are being used.

5.2 TEST PROGRAM

As a result of the Task I studies conducted to date, we believe that the maximum amount of significant information can be obtained from the Device Performance Evaluation Phase if its objectives are to determine:

A. The degree to which a comparatively sensitive. microcircuit is prone to degradation by surface charge accumulation;

B. The effectiveness of the glass encapsulation in the prevention of sufficient surface charge accumulation to cause channels, even when the package is non-hermetic;

C. Whether glassing the microcircuit is deleterious in any respect to circuit reliability.

To achieve these objectives, three hundred (300) revised test vehicle microcircuits will be submitted to the Reliability and Quality Control Department for appropriate tests, as described below.

These 300 units will be selected from about 500 assembled on the basis of initial electrical characterization. The 300 units will be divided into four(4) groups with the following approximate distribution:

A. Glassed

1) Sealed ≈ 75
2) Open ≈ 100

B. Unglassed

1) Sealed ≈ 65
2) Open ≈ 60

There may be an additional small number of units with field plate encapsulation over the glass, sealed and open.

The electrical parameters which will be measured on these devices are shown in Table 6.

Because the total quantity of devices involved is large, automatic parameter test equipment will be used to facilitate the measurements. The use of the automatic equipment, however, will not permit measurement of beta at a constant collector current because a constant voltage and current cannot be simultaneouly programmed to the same device pin. Therefore, the beta measurements will be made at a constant I_B rather than the conventional constant I_C. Also, the lowest current measuring range is 100 nA to 10 μA with an accuracy of ±100 nA. Although this is not low enough to read the junction leakage of "good" devices, it is adequate to determine the existence of inversion layers.

The schedule of environmental and long term operational tests which is most likely to fulfill the objectives of the program, based on the understanding gained from the initial phases of the program is shown below.

TABLE 6

ELECTRICAL PARAMETERS AND TEST CONDITIONS FOR REVISED VEHICLES*

Parameter**	Component	Conditions	Measure	Units
1. I_{RGO}	Resistor-Isolation	Pin 2 = 10ω; Pin 4 = Gnd	I at Pin 9	μA
2. I_{IRO}	Isolation-Resistor	Pin 4 = 10ω; Pin 9 = Gnd	I at Pin 4	μA
3. I_{BRO}	Base-Resistor	Pin 4 = 10ω; Pin 2 = Gnd	I at Pin 4	μA
4. I_{RBO}	Resistor-Base	Pin 2 = 10ω; Pin 4 = Gnd	I at Pin 2	μA
5. I_{GBO}	Isolation-Base	Pin 2 = 10ω; Pin 9 = Gnd	I at Pin 2	μA
6. I_{BGO}	Base Isolation	Pin 9 = 10ω; Pin 2 = Gnd	I at Pin 9	μA
7. I_{RCO}	Resistor-Collector	Pin 1 = 10ω; Pin 4 = Gnd	I at Pin 1	μA
8. I_{CBO}	Test Transistor	Pin 1 = 10ω; Pin 2 = Gnd	I at Pin 1	μA
9. I_{CGO}	Collector-Isolation	Pin 1 = 10ω; Pin 9 = Gnd	I at Pin 1	μA
10. I_{CEO}	Test Transistor	Pin 1 = 10ω; Pin 14= Gnd	I at Pin 1	μA
11. I_{ECO}	Test Transistor	Pin 14 = 1ω; Pin 1 = Gnd	I at Pin 14	μA
12. I_{EBO}	Test Transistor	Pin 14 = 5ω; Pin 2 = Gnd	I at Pin 14	μA
13. Beta	Test Transistor	Pin 1=5V;Pin 2=1μA;Pin 14=Gnd	I at Pin 1	μA
14. Beta	Test Transistor	Pin 1=5V;Pin 2=10μA;Pin14=Gnd	I at Pin 1	mA
15. I_{CBO}	Control Transistor	Pin 10 = 10V; Pin 7 = Gnd	I at Pin 10	μA
16. I_{CEO}	Control Transistor	Pin 10 = 10ω; Pin 8 = Gnd	I at Pin 10	μA
17. I_{ECO}	Control Transistor	Pin 8 = 1ω; Pin 10 = Gnd	I at Pin 8	μA
18. I_{EBO}	Control Transistor	Pin 8 = 5ω; Pin 7 = Gnd	I at Pin 8	μA
19. Beta	Control Transistor	Pin10=5V;Pin 7=1μA;Pin 8=Gnd	I at Pin 10	μA
20. Beta	Control Transistor	Pin10=5V;Pin 7=10μA;Pin8=Gnd	I at Pin 10	mA
21. $I_{C_1C_2O}$	Collector-Collector	Pin 1 = 10ω; Pin 6 = Gnd	I at Pin 1	μA
22. $I_{C_2C_1O}$	Collector-Collector	Pin 6 = 10ω; Pin 1 = Gnd	I at Pin 6	μA
23. I_{C_6GO}	Collector-Isolation	Pin 6 = 36ω; Pin 9 = Gnd	I at Pin 6	μA
24. $Beta_I$	Test Transistor	Pin 14=1ω;Pin 2=10μA;Pin 1=Gnd	I at Pin 10	μA
25. $Beta_I$	Test Transistor	Pin 14=1V;Pin 2=20μA;Pin 1=Gnd	I at Pin 10	μA

TABLE 6 (CONTINUED)

Parameter**	Component	Conditions	Measure	Units
26. BV_{CBO}	Test Transistor	Pin 1=100μA(Positive);Pin 2=Gnd	V at Pin 1	V
27. I_{L_3}***	Surface Plate-Isolation	Pin 1,2,4,5,6,7,8,9,10,12 and 14=Gnd; Pin 3 = +36V	I at Pin 3	μA
28. I_{L_5}***	Surface Plate-Isolation	Pin 1,2,3,4,6,7,8,9,10,12 and 14=Gnd; Pin 5 = +36V	I at Pin 5	μA
29. I_{L-12}***	Surface Plate-Isolation	Pin 1 = Gnd; Pin 12 = +1V	I at Pin 12	μA
30. I_{L-11}***	Field Plate-Isolation	Pins 1,2,3,4,5,6,7,8,9,10,12 & 14=Gnd; Pin 11 = +36V	I at Pin 11	μA

* Since the surface plates on these devices are floating, the units must be handled with the same precautions used with MOS devices to avoid discharge of electrostatic charge.

** The subscripts used are:

E = Emitter Region
B = Base Region
C = Collector Region
R = Resistor Region
G = Isolation Region
F = Field Plate
L = Surface Plate

*** These parameters need only be measured initially to guarantee isolation of surface and field plates.

The units will be subjected sequentially to the following four tests. All parameters listed in Table 6 will be measured following each test.

A. Temperature

1. Storage (16 hours at 200° C stabilization bake).

   Test 100% of units.

2. Cycling (MIL-STD-750 Method 1051.1; -55° C to +200° C air to air; at temperature 1/2 hr).

   Test 100% of units.

3. Thermal Shock (MIL-STD-750 Method 1056.1, Test Condition B, except temperatures to be -55° C to +200° C liquid to liquid).

   Test all sealed units.

B. Vibration (MIL-STD-750 Method 2056 except G level to be 30G).

   Test 100% of units.

C. Mechanical Shock (6000G in Y_1 & Y_2 planes 0.5 ms).

   Test 100% of units.

D. Acceleration (MIL-STD-750 Method 2006 except only in Y_1 and Y_2 planes; 20,000G (not encapsulated)).

   Test 100% of units.

Following these tests, ten units of each of the four types will be submitted to:

E. 10-day moisture tests (MIL-STD-750 Method 1021.1) without bias applied. The units will be baked 1 hr at 125° C to drive off excess water to avoid electrolytic attack of the metalization during parameter measurement. If no failures exist after this test, the units will be subjected to the same test with bias applied as in F below (except no bias will be applied to Pin 6), and measurements taken each day until ten more days have been completed.

F. Operational Life: All units from D which did not go into E will be divided in two groups for long term (4000 hr) operational life testing at 25° C or 75° C. The conditions will be as follows:

Conditions	
Pin 2	= -5V
Pin 5, 9, 11, and 14	= Gnd
Pin 1, 3, and 12	= +10V
Pin 6	= +36V

The units at 25° C will be removed from the test a rack at a time to minimize delay between test and parameter measurement. The units at 75° C will be cooled under bias for about 10 minutes before removal of bias and measurement.

Parameter measurements will be obtained at about 0, 250, 500, 1000 and 4000 hours.

5.3 DEMONSTRATION MODELS

Fifty-five devices demonstrating the incorporation of the glassing process on actual circuits will be submitted. These devices will be PA7709 circuits, although they will not be tested to meet all commercial specifications. Five of these devices will be left open to permit visual inspection and evaluation of the glassing technique.

SECTION 6 - PROGRAM FOR THE NEXT INTERVAL

During the next quarterly period the assembly and selection of units for the performance evaluation will be completed and the units will be submitted for the test program. Data from the environmental and life test program will become available and will be discussed in the Final Report.

The specification for the encapsulation material and the procedure for encapsulation will be prepared and included as part of the Final Report.

Demonstration models will be supplied consisting of a basic analog microcircuit similar to the unit used for the revised test vehicle.

Some additional tests will be made to further verify the present understanding of device stability.

APPENDIX

MATERIALS STUDY

Purpose

The purpose of this study was to determine the optimum characteristics of the material to be used for the glass encapsulation of semiconductor devices.

Introduction

Glass encapsulation must chemically and physically protect semiconductor devices from their environment to prevent both progressive and catastrophic degradation of the functional properties of those devices.

In view of this requirement, any glasses which would be potentially useful as encapsulants would be those which, in the form of thin deposits, have the following characteristics:

(1) Are insulators of high dielectric strength:
(2) Are rigid, inert, and stable:
(3) Are crystallographically and structurally compact and, as such, not amenable to the formation of pinholes, porosity, or to transverse ion migration.

It is not expected that all possible materials for glass encapsulation will possess all these characteristics to a high degree. Instead, a certain amount of "trading-off'' of characteristics can be expected.

Certain practical considerations limit the number of potentially useful materials that could be employed as encapsulants. For example, it is economically desirable to apply the glassing material to wafers rather than individual devices to which bonded connections have already been made. However, if the glass is applied to the wafers, it must be delineated and etched to permit connections to be made at some later time. Therefore, the material must be etchable.

Furthermore, if an elevated temperature is necessary for the deposition of the glass film, then that temperature must not be so high as to have an irreversible, deleterious effect upon the wafer. Since Al metalizations are quite often used on Si devices, the upper temperature limit of a wafer containing such devices must be below the Al-Si eutectic temperature, which is 577°C[1].

Finally, the existing technology governing the deposition of a given material by a given process must be so advanced as to permit the deposition of the required thickness within a practical time.

Taking the above considerations into account, it was concluded that the greatest success would be obtained by using the low temperature oxidation of silane, or one of its modifications. Alternative processes of interest would be electron beam evaporation or r-f sputtering of such materials as silica, alumina, or mullite.

The Material and Its Method of Deposition

The objectives of glass encapsulation will be realized with the greatest amount of success if SiO_2 deposited by the silane process is used as the protective glass layer. While this glass technique may not perform every function of a protective layer better than any other material or deposition technique, it is the best method available at the present level of solid-state technology. The selection of the silane process is a result of considering the design requirements and trade-offs of characteristics among the competing techniques for glass encapsulation. On the whole, the silane process will provide semiconductor devices with chemical and physical protection from their environment better than any other glassing technique.

The characteristics of SiO_2 deposited by the silane process which led to the above conclusions are:

1. It is completely compatible with all the device processing steps that precede it in time; the temperature required for the deposition process is lower than any critical temperature that is generally characteristic of semiconductor devices.

2. It results in a layer of high resistivity and low dielectric constant with a perfectly adequate dielectric strength.

3. It results in uniform thickness deposits over large areas and has the ability to coat the sides of topographical features as well as the tops.

4. The glass layers have very low pinhole densities.

5. The deposits are sufficiently rigid to provide a high level of mechanical protection to the metalizations.

6. The deposits have etching chracteristics that permit the delineation and etching of cuts to the contact pads of underlying metalizations.

7. The glass layers are stable over extremely long periods of time.

8. The layers contain a very low level of contamination.

9. The deposition rates that can be obtained result in very reasonable times for the deposition step.

Other advantages of the silane deposition system are:

1. The technique is already well enough developed to permit its incorporation into a production system.

2. The technique is economical, both in terms of capital equipment required by the deposition system, and the expendable materials that the deposition system consumes.

3. The manipulation of the deposition system requires minimal operator training and can be automated if necessary.

The only drawback to using Si02 deposited by the silane process is ion migration. Specifically, a deposited layer of Si02 from silane will not inhibit the migration of ions either already in the deposit, or brought to the surface. However, this problem can be solved if phosphosilicate glass is present in the system as it generally is for bipolar processes, Tests have shown it will act as an efficient sodium and hydrogen ion getter. In the case where phosphorus is not used in the basic process, then a thin deposit of phosphosilicate glass can be formed on top of the silane vapor plated glass. The phosphosilicate glass will getter the undesirable ions, and minimize the one weak characteristic that silane deposited Si02 shares with glass deposited by other techniques.

A thorough specification of the glass encapsulating layer requires, among other things, a discussion of the thickness that it should have.

Thickness

In determining the optimum thickness for a glass passivating layer, consideration of the need for physical and chemical protection alone indicates that the thicker a layer is, the more protection it will provide.

For example, as thickness increases, the surface pinhole density of deposited glasses decreases. Furthermore, the adverse effects of a constant level of porosity and pinholes decrease as the thickness increases.

The method of deposition being considered can be classified as a molecular deposition technique. In this technique, the sides of specimen details are coated as well as the tops. Other deposition techniques are characterized by the straight-line transfer of material from source to substrate: surface details in this case produce the phenomenon of shadowing. Although the sides of details are coated during a molecular deposition technique, they are probably not coated quite as thickly as the top horizontal surfaces. Since the major topographical features of an integrated circuit are the metalizations, these thin side coatings represent potential short circuits. This potentiality can be avoided if the glass layer is made at least as thick as the metalizations, that is, the glass coating should be at least 10,000 Å thick.

Also, the abrasion resistance of the glass will be greater for greater thicknesses. Since this quality will be useful in preventing scratches in the soft Al metalizations, here again it is advisable for the glass layer thickness to be at least as great as the thickness of those metalizations. Scratches in the Al metalizations, even when they do not result in open circuits, produce a high resistance which ultimately can result in failure.

Finally, the dissolution of metalizations due to electrochemical cell action has been observed to occur on integrated circuits when they are exposed to a moist environment. If a glass encapsulating layer is expected to retard such electrochemical action, then the thicker the glass layer is, the greater will be the retardation.

However, in determining the optimum thickness of the glass layer, there are several considerations, in addition to those of physical and chemical protection, that must be taken into account. These are (1) stray capacitances from metalizations to a field plate (when a field plate is used); (2) the precision of delineation of holes in the glass layer: (3) the accuracy of etching contact cuts of a given depth without excessive etching of the underlying metalization; and (4) the stress in the glass film.

1. Stray Capacitance

In certain situations it may be desirable to use a field plate (large geometry conducting film) over the glass encapsulating layer of an Lntegrated circuit. Such a measure can be employed to prevent a lateral electric field from existing at the ambient-dielectric interface. In the absence of a lateral field, lateral surface ion migration will not occur, This is true whether the ambient is a gas in a hermetically sealed package, room air over an unsealed device, or plastic over a coated substrate containing active devices or circuits. Another application of the field plate is to cause mobile ions having a specific charge, which are found in the glass layer, to migrate toward the plate rather than toward the device. This could be accomplished by the application of a suitable bias to the field plate. It would be useful if specific ions were known to produce an undesirable effect at the device surface.

However, the stray impedance which will exist between the metalizations and a field plate of this nature will limit the frequency response of the integrated circuit. The stray impedance will have a component due to the resistance of the glass dielectric which will be in parallel with a component due to the capacitance between the metalizations and the field plate. Thus, if Z_s is the stray impedance, then

$$\frac{1}{Z_s} = \frac{1}{R_g} - \frac{1}{jX_{c,g}} \quad ,$$

where R_g is the resistance due to the glass, and $X_{c,g}$ is the capacitive reactance due to it. A complete transient analysis of the problem would require a specific knowledge of the harmonic components of the input signal to the integrated circuit as well as the impedance characteristics of the devices in the circuit. However, a rough approximation based on a very simple model is all that. is required at this point. Consider a short length of metalization, ℓ, of width w which has been covered with a glass layer of thickness t_g, as in Figure 1. If we assume that the

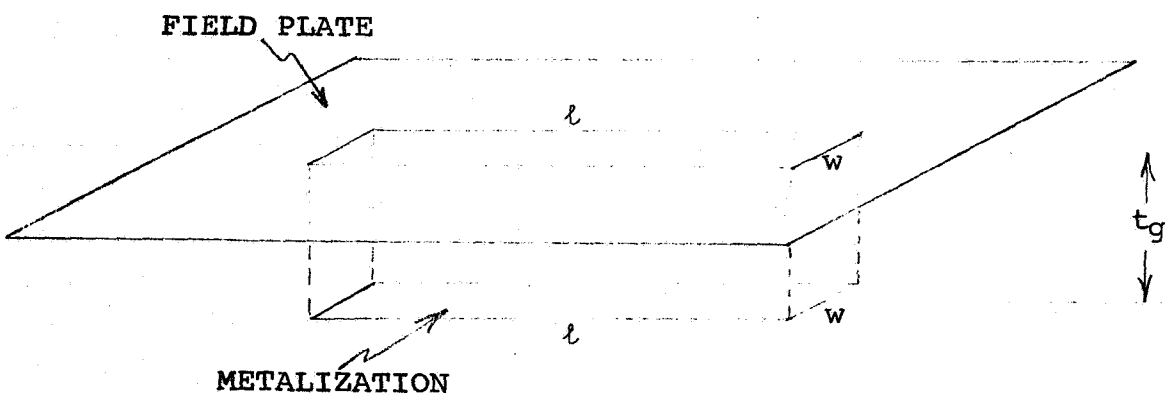

Figure 1.

parallel resistance and capacitance of the dielectric layer arise only from the dielectric within the volume of the metalization and its normal projection on the field plate, then we have

$$R_g = \rho_g \frac{t_g}{\ell w} ,$$

where ρ_g is the resistivity of the glass, and

$$X_{c,g} = \frac{1}{\omega C_g} \quad \frac{t_g}{\omega K_g \epsilon_o \ell w}$$

where C_g is the "parallel plate" capacitance of the metalization and the field plate, ω is the frequency, K_g is the dielectric constant of the glass, and ϵ_o is the permittivity of free space. Therefore, to prevent serious degradation of the response of the integrated circuit, in general the stray impedance, Z_s, must be as large as possible. By inspection, it is apparent that a high Z_s is obtained when

(a) the design parameters

(1) ℓ and w are as small as possible, and
(2) t_g is as great as possible:

and (b) the material parameters

(1) ρ_g is as great as possible, and
(2) K_g is as small as possible.

2. Delineation

The method by which openings will be generated in the glass film for purposes of electrical connection will be etching through photoresist masks. An important consideration when etching through masks is that the lateral etch rate is approximately equivalent to the transverse etch rate. Because of this, the thicker a film is relative to the dimensions of the opening, the less faithful the final opening dimensions will be relative to the original mask. However, the degree of fidelity required when cutting through glass passivating layers is not as great as that required when delineating structures beneath the glass layer. In fact, an expected error of about 5% can probably be

tolerated. This is the situation when the narrowest opening dimension is forty times greater than the glass film thickness. Under these conditions, an opening with a narrowest dimension of 5 mils (125 μ) will limit the maximum glass thickness to 3.1 μ. But, if either the etch geometry error or the dimensions of the openings are required to be less than the values that were assumed, then the maximum tolerable glass thickness will be correspondingly lower.

3. Etch Depth Accuracy

The etchant which is used to generate the openings in glass layers is a selective etchant, in that its etch rate for films of glass is relatively greater than its etch rate for evaporated metals of the kind to which contacts must be made. However, in practice, true etchant selectivity is not obtained. There are several reasons for this. When an adherent glass film is deposited on a metalization, a certain amount of solid-state chemical reaction takes place at the glass-metal interface. In fact, such a reaction is necessary for good film adherence. Although the extent of such a reaction is limited in terms of bulk dimensions, it can be significant in terms of film dimensions. Its effect in terms of the problem here is to so modify the etching characteristics of the chemically reacted metal that they tend to become more similar to those of the glass. Since etchants cannot be considered to be absolutely selective, the etching time, t, must be controlled to etch openings in glass films of a given thickness, d. If the rate of etching that has been empirically determined is r, then we have

$$rt = d.$$

If ϵ_r is the fractional error involved in knowing the etch rate of the material (due to point-to-point inhomogeneity across a wafer), and ϵ_d is the fractional error in d due to thickness non-uniformity of the glass film, then there will be a fractional error, ϵ_t, induced in the time required for etching,

$$r(1 + \epsilon_r)t(1 + \epsilon_t) = d(1 + \epsilon_d),$$

or $$(1+ \epsilon_r)(1 + \epsilon_t) = (1 + \epsilon_d).$$

Therefore, $$\epsilon_t = \frac{\epsilon_d - \epsilon_r}{1 + \epsilon_r}$$

Since the errors in etch rate and film thickness can be either positive or negative, then the maximum error in time, which is realized when a sample is etched sufficiently long to remove the thickest and most etch-resistant regions, is

$$\epsilon_t = \frac{|\epsilon_d| - |\epsilon_r|}{1 - |\epsilon_r|} .$$

The absolute error in the etch time, At, will be

$$a t = \epsilon_t t = \epsilon_t \frac{d}{r} .$$

Thus we see that the absolute error in etching time, At, besides depending on the etch rate error and thickness non-uniformity, also depends on the thickness of the glass layer. The probability of etching the underlying metalization increases with At, and therefore with d, the thickness of the glass.

It is difficult to quantitatively correlate considerations such as these with a maximum glass thickness. Therefore, it must suffice to conclude that these considerations will limit the maximum film thickness that is practical, and that in general, increases in film thickness will adversely affect the etch depth accuracy.

4. Stress

Glass films, as they are deposited, are generally found to be under stress at room temperature. In fact, films in general, whether metal, semiconductor, or dielectric, are rarely, if ever, deposited in a stress-free condition. The stress in glass films, however, limits the thickness to which they can be deposited. Beyond this thickness, the films rupture,

At Philco-Ford, films of Si02 have been deposited by means of the silane process onto thin and flexible (111) Si wafers to observe the stress. During deposition, the substrates warped concavely as viewed from the film side, indicating the film was under tension. They remained warped even after they cooled to room temperature. This stress limits the maximum thickness of SiO_2 which can be deposited on a non-deformable Si wafer by this process to between 1.5 and 2.0 μ.

Investigations of the factors associated with stress in films have mainly dealt with metal films formed by vacuum evaporation. These factors, nevertheless, have a great deal of relevance to glass dielectric films produced by either chemical techniques or r-f sputtering. The factors which produce or affect the stress in films are:

1. The thermal coefficients of expansion of the film and the substrate. When a film is deposited at an elevated temperature, differential thermal contraction between film and substrate will produce a stress in the film as it cools to room temperature. This type of stress is reversible.

2. The recrystallization temperature of the film material[2]. When a material such as a metal is evaporated onto a substrate, condensation takes place at a temperature which is generally greater than room temperature. Since the state of thermal expansion of the condensate is characteristic of that temperature, whereas that of the substrate might be much lower, then when the condensate contracts upon cooling it will become stressed. This type of stress is also reversible.

3. Crystalline imperfections, vacancies and dislocations[3]. The crystalline lattice in the vicinity of a vacancy is distorted inwardly toward the vacancy, that is, the vacancy produces a tensile stress in the lattice. Dislocations, on the other hand, cause the lattice to be in a somewhat expanded state. They produce a compressive stress in the lattice. Other imperfections may also produce stresses. These stresses are irreversible in the sense that they can not be annealed out.

4. The angle of incidence of the vapor beam during deposition[4], This factor pertains to unidirectional deposition techniques such as evaporation.

5. The residual gas composition during deposition[2].

6. The absorption of gases after evaporation[5].

7. Surface tension and compression effects[6]. Films that are still in the island stage of development exhibit stress which is partly due to the surface tension of the islands and partly due to the cohesive forces between the islands.

8. Voids and porosity. When voids are occluded in films with a positive surface tension, the net effect is a tensile stress because the lattice is distorted in toward the voids. Porosity can similarly produce stress in films.

9. Lattice mismatch[7]. A factor contributing to the stress in epitaxial heterogeneous overgrowths.

For glass films produced by the silane process, the important factors associated with stress are differences in thermal expansion coefficients, the residual gas concentration during deposition, and voids and porosity in the resultant film. The first factor is important because the silane process requires that the films be formed at elevated temperatures on substrates also at elevated temperatures. The second reason is generally an important one in systems that involve oxygen. When the deposition conditions are modified so as to affect the stoichiometry of the glass film, then any such modification which favors the oxygen content of the film will increase the compression of the resultant films and vice versa. The third reason can be expected to be important because the glass films by the silane process are generally less dense than bulk SiO_2.

Recrystallization temperature effects and crystalline imperfections, voids, and dislocations are usually very important factors associated with the stress in films. Although they are usually the most important causes of stress in metal films, they are crystallinity-dependent factors, and as such rather insignificant when considering the stress in glass films.

It may be desirable to change the stress in glass films for several reasons. Obviously, if the upper limit of thickness of a glass film due to stress becomes objectionable, it may be desirable to form glass films with less or, if possible, no stress in them. On the other hand, assuming that a perfect match of coefficients of expansion between film and substrate cannot be obtained, then even a zero initial stress might not be favorable. The most favorable thing might be to incorporate an initial compressive stress in the glass film. Depending upon just what the differential expansion between film and substrate is, such a measure could be used to compensate for an anticipated dimensional incompatibility at either elevated temperature storage or operation. The previous comments concerning stress in glass films indicate that the modification of the proportion of reactants is probably the easiest way to produce a change in the stress of a given film. Changing the void content or the porosity of a film will probably not be quite

as easy. Likewise, to change the thermal coefficient of expansion of a film so as to match the substrate would be quite 'difficult, if not impossible. However, the latter can be accomplished if the film itself is changed. This possibility is discussed in the next section.

Compatibility of Thermal Coefficient of-Expansion

When it is necessary to change the thermal coefficient of expansion of a glass film it can be accomplished by introducing a new component to the glass system. In a binary glass system the thermal coefficient of expansion will be a function of the composition. If the system is chosen properly, then almost any desired coefficient of expansion can be obtained at some concentration within the limits of the pure components.

The thermal coefficient of expansion of a polycrystalline material is a structure-insensitive property; that is, it does not depend upon grain size or other structural properties of a material. In binary isomorphous or eutectic systems, the values of such properties do not have extrema beyond the values of the pure component limits. On the other hand, structure sensitive properties such as hardness do. The same comments are true for systems that tend to be amorphous. Eitel[8] states that in the case of glasses, since they are "solidified melt solution", that many physical properties of oxide glasses of more than one component can be determined by a summation expression of the type

$$X = a_1y_1 + a_2y_2 + a_3y_3 \quad \ldots\ldots\ldots\ldots$$

where the y_i are the composition fractions of the various components of the glass system, and the a_i are constants which depend upon the physical property being considered and the particular glass system in question. He also states that the thermal coefficient of expansion is a property that possesses such a dependence upon composition.

Since the literature value of the linear thermal coefficient of expansion of Si is $4.2 \times 10^{-6}/^{\circ}C$, whereas the value for fused silica is only $0.54 \times 10^{-6}/^{\circ}C$, it might appear that the two materials have mismatch problems. However, since the same property for Al_2O_3 is $7.2 \times 10^{-6}/^{\circ}C$, then it might be possible to form a material of composition $(SiO_2)_x(Al_2O_3)_y$ that has a coefficient of expansion equal to that of Si.

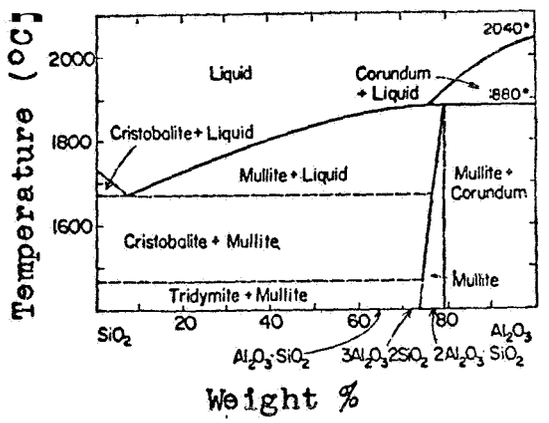

Figure 2.

Figure 2 is the equilibrium phase diagram for the binary system SiO_2 - Al_2O_3 (9). Below about 850° C down to room temperature, the stable crystallographic configurations of SiO_2 are the low and high modifications of quartz. However, it is the vitreous modification of these materials that is relevant to glass encapsulation. The films obtained from the straight-forward silane process would be expected to have properties analogous to those of fused silica, and from all indications the compound Si02 - Al_2O_3 films that can be obtained from a modification of that process will also be vitreous as determined bv glancing angle electron diffraction.

Although thermal coefficient of expansion data is available for fused silica, it is not available for vitreous $3Al_2O_3 \cdot 2SiO_2$ or vitreous Al_2O_3 because these materials have not been obtained in bulk form in the vitreous state. They possess a strong tendency to crystallize from the melt even with rapid cooling.

However, as an approximation, the data that is available for polycrystalline mullite and polycrystalline alumina can be used in the calculation of the thermal coefficient of expansion as a function of composition in the Al_2O_3 - SiO_2 system.

In a binary system with components a and b, the volume thermal coefficient of expansion, γ, is

$$\gamma = v_a\gamma_a + v_b\gamma_b \ ,$$

where v_i is the volume fraction of component i and γ_i is its volume thermal coefficient of expansion. Using the approximation that the linear thermal coefficient of expansion α is equal to 1/3 the volume coefficient of expansion, we have

$$\alpha = \frac{1}{3}\gamma = \frac{1}{3}v_a\gamma_a + \frac{1}{3}v_b\gamma_b$$

$$= v_a\alpha_a + v_b\alpha_b \ ,$$

where α_i is the linear thermal coefficient of expansion for component i. Since

$$v_i = \frac{\frac{n_iM_i}{d_i}}{\frac{n_iM_i}{d_i} + \frac{n_jM_j}{d_j}} \ ,$$

where n_i is the mole fraction of component i, and M_i and d_i are its molecular weight and density, respectively, then one can write

$$\alpha = \frac{\alpha_a(n_aM_a/d_a) + \alpha_b(n_bM_b/d_b)}{(n_aM_a/d_a) + (n_bM_b/d_b)}$$

Using this relationship between the limits SiO_2 and $3Al_2O_3 \cdot 2SiO_2$ for which the linear thermal coefficients of expansion are $0.54 \times 10^{-6}/°C$ and $5.3 \times 10^{-6}/°C$, respectively, and then between the limits of $3Al_2O_3 \cdot 2SiO_2$ and Al_2O_3 for which they are $5.3 \times 10^{-6}/°C$ and $7.2 \times 10^{-6}/°C$, respectively, we obtain the curve in Figure 3. As pointed out, this curve is only valid as an approximation. The thermal coefficients of expansion for glassy

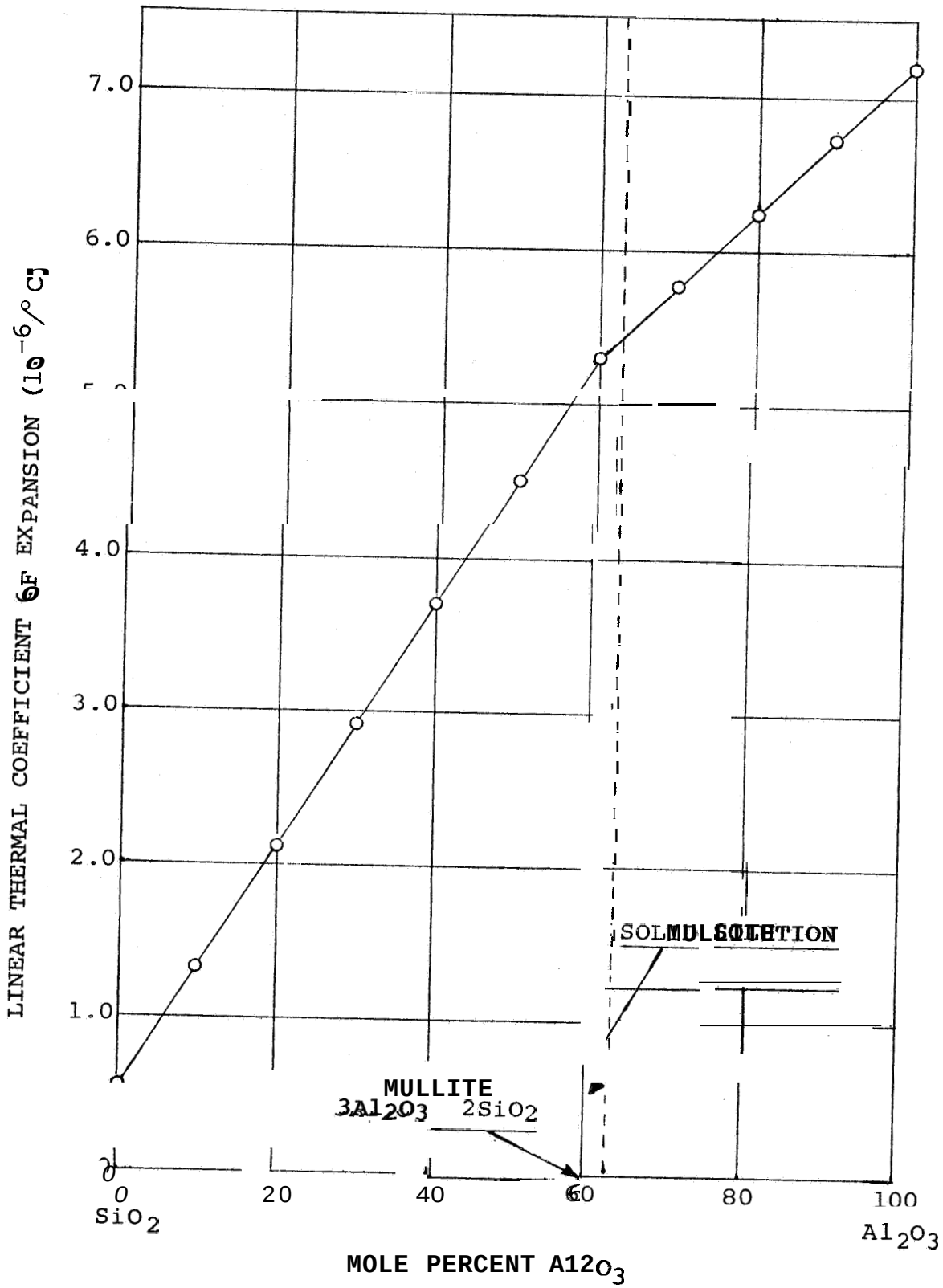
LINEAR THERMAL COEFFICIENT OF EXPANSION (10^{-6}/°C)
7.0
6.0
4.0
3.0
2.0
1.0
SOLID SOLUTION
MULLITE
$3Al_2O_3$ $2SiO_2$
0
20
40
60
80
100
SiO_2
Al_2O_3
MOLE PERCENT Al_2O_3

FIGURE 3

$3Al_2O_3 \cdot SiO_2$ and glassy Al_2O_3 may actually be lower than the values that were assumed. Nevertheless, the data has utility as a guide to the tailoring of a material that has a given desired thermal coefficient of expansion.

Surface Preparation

Given a glass film with a linear thermal coefficient of expansion that is perfectly compatible with the substrate, there is still a problem that might exist. In particular, it is the problem of poor adherence of the film to the substrate. This is a problem that tends to be more critical for thick films that for thin ones, since small stresses in films account for greater forces in thick films than in thin ones. These forces, then, would cause the film to be sheared free of the substrate.

The factors which have been found to affect the adhesion of films to substrates are:

1. The materials of the film-substrate pair, [10]
2. The oxide which forms at the film-substrate interface, [11]
3. The contamination of the substrate, [11]
4. The aging of films which have been deposited on unheated substrates [12] or the deposition of films on substrates at elevated temperatures. [11].

The materials in question are deposits of glass and substrates with top surfaces of both thermally grown SiO_2 and a metal - most probably Al. It is not expected that this combination of materials will pose adhesion problems in itself.

Good adhesion between film and substrate is obtained when there is a continuity between the structure of the substrate and the film. This usually occurs via an interfacial oxide. For example, for metals deposited on oxide substrates such as silica or alumina, the greater the tendency of the metal to form an oxide, that is the larger its negative free energy of formation of oxide, the greater will be its adhesion to the substrate. [11]

From this point of view, glass deposits are expected to have good adhesion to Al since the free energy of formation of Al_2O_3 is -376.77 kcal./mole, which is high compared to most metals. In reality, Al films on glass are somewhat anomolous [12]. They do not possess the adhesion that a large negative free energy of formation of the oxide suggests. However, Al adhesion to glass is not poor; it is usually found to be greater than the adhesion of metals such as Cu and Cd to glass; and it is always much greater than the adhesion of metals such as Ag and Au. Furthermore, the

aging of Al films on glass in air at room temperature dramatically improves their adherence.[12] This observation suggests that the formation of the oxide layer is not complete at the time of deposition, but in fact continues even during storage at room temperature.

There have been no reports in the iiterature concerning the adhesion of glass films to oxide substrates. However, on the basis of the free energy of formation of SiO_2 which is -190.9 kcal./mole, adhesion problems resulting from the lack of an interfacial transition region are not expected. This has been borne out by the experience at Philco-Ford. Although no quantitative determinations were made of the adhesion of SiO_2 films formed by the silane process, nevertheless, no indications of poor adherence were encountered,

The substrate temperature during deposition is another factor that can influence adhesion. The deposition of a film onto a heated substrate, as opposed to a substrate at room temperature, will tend to increase the adhesion of the film[11] if the elevated temperature promotes oxide formation at the film-substrate inkerface.

The contamination of a substrate surface can degrade the adhesion of a film to that surface. The exact degree of cleanliness or contamination of a surface is difficult to establish. However, films deposited on substrates that are improperly cleaned do adhere poorly.[11] Furthermore, severe contamination of a substrate produces major and sometimes total loss of adhesion.

A surface preparation step that could be used to increase the adhesion of a glass coating to thermal SiO_2 is the formation of a phosphosilicate glass top layer by means of phosphorus diffusion. This would increase the adhesion of a glass deposit for two reasons. First, the SiO_2-P_2O_5 system forms a eutectic at approximately 15 mole percent P_2O_5 with a eutectic temperature of about 970° C.[13] This is much lower than the melting point of pure SiO_2. It is expected that structural continuity between deposit and substrate can be realized by an annealing process as well as by an oxidation process at the interface, and the annealing step is more likely to occur if the liquidus temperature of the components can be decreased. Obviously, a heat treatment would facilitate interfacial continuity, whether it resulted from annealing or oxidation.

The second reason that the adhesion of a glass deposit would be increased by the formation of a phosphosilicate glass top layer is that phosphosilicate glass tends to be hydrophilic. Since

moisture lowers the annealing point of glasses, then interfacial oontinuitycould be attained by annealing at a low temperature during deposition or during a separate annealing step. If a phosphosilicate glass layer is used, care must be taken to avoid the presence of excess water at the interface during glass deposition. An excess of water would destroy glass adhesion. However, a simple bake could be used to arrive at the most suitable surface moisture level.

Another surface treatment that could be used to increase glass-deposit adhesion is the elevated temperature drive-in of a fluxing agent such as B_2O_3. Again, interfacial continuity would be attained by an annealing process. The borosilicate system would be expected to anneal at about 600° C. The resulting adherence properties would be the same as if a borosilicate glass were deposited initially. Such a deposit could be chemically vapor plated by means of the oxidation of silane with triethylboron alkyl. (14)

Summary

Table I is a capsule recapitulation of the foregoing discussion. In view of the comments in Table I, the optimum thickness range of a glass encapsulating layer of SiO_2 deposited by the oxidation of silane process is 10,000 to 15,000 Å. To minimize leakage and stray capacitance, the resistivity of the layer should be as high as possible and its dielectric constant as low as possible.

The thermal coefficient of expansion of the glass layer is not an imminent problem. However, the versatility of the silane process permits additional reactants to be admitted to the oxidation chamber. In this way, binary or multi-component glasses of any composition can be deposited. With proper selection, the thermal coefficient of expansion could be tailored, within limits, to a desired value.

Finally, glass encapsulating layers are expected to adhere well. If phosphosilicate glass layers that have been deposited for the purpose of ionic gettering have any effect at all on adhesion, the effect will tend to be one of enhancing the adhesion.

TABLE I.

ITEM	COMMENT
Surface pinhole density	Glass should be as thick as possible.
Porosity	do.
Stray capacitance	do.
Complete coating of the device including the vertical sides of details as well as the top surfaces	Glass should be at least 1 μ. thick (the thickness of the metalizations), preferably thicker.
Abrasion resistance	do.
Precise delineation of holes through glass	Glass should be no thicker than 3.1 μ for 5% accuracy and 5 mil holes.
Stress in the glass films	Glass cannot be thicker than 1.5 to 2.0 μ. This limitation will be removed by properly adjusting the experimental deposition conditions. It should be possible to incorporate a given amount of either tensile or compressive stress, if desired.
Accuracy of etching contact cuts of a given depth without excessive etching of the underlying metalization	Glass must not be too thick.
Leakage	The resistivity of the glass should be as high as possible.
Stray capacitance	The dielectric constant of the glass should be as low as possible.
Thermal coefficient of expansion	Should it be desired, the value of this property can be modified within limits by introducing a second component to the glass system.
Adhesion	No problems are anticipated provided surfaces are free of contamination and excess moisture. However, adhesion will be increased if phosphorus glass or a fluxing agent is used.

REFERENCES

1. Hansen, M., Constitution of Binary Alloys, McGraw-Hill Book Co., Inc., New York, 1958, p. 133.

2. Murbach, H.P. and Wilman, H., Proc. Phys. Soc., B66, 905 (1953).

3. Hoffman, R.W., Anders, F.J., and Crittenden, Jr., E.C., J. Appl. Phys., 24, 231 (1955).

4. Finegan, J.D. and Hoffman, R.W., Vac. Symp. Trans., 1961, 936, Pergamon Press, London, 1962.

5. Priest, J.R. and Caswell, H.L., Brit. J. Appl. Phys., 12, 580 (1961).

6. Heavens, O.S. and Smith, S.D., J. Opt. Soc. Am., 47, 469 (1957).

7. Chikazumi, S., J. Appl. Phys. Suppl. 32, 81S (1961).

8. Eitel, W., The Physical Chemistry of the Silicates, The University of Chicago Press, Chicago, 1954, p. 1326.

9. Levin, E.M., Robbins, C.R., McMurdie, H.F., Phase Diagrams for Ceramists, The American Ceramic Society, Columbus, Ohio, 1964, p. 122.

10. Benjamin, P. and Weaver, C., Proc. Roy. Soc., A254, 163 (1960).

11. Karnowsky, M.M. and Estill, W.B., Rev. Sci. Instr., 35, 1324 (1964).

12. Benjamin, P. and Weaver, C., Proc. Roy. Soc., A261, 561 (1961).

13. Levin, E.M., Robbins, C.R., McMurdie, H.F., Phase Diagrams for Ceramists, The American Ceramic Society, Columbus, Ohio, 1964, p. 142.

14. Evitts, H.C., Tolliver, D.L., and MacKenzie, K.R., "Large Area Semiconductor Surface Passivation Production Refinement Program", Technical Report AF'ML-TR-65-285, prepared under Contract AF33(657)-11268 by Motorola, Inc., Phoenix, Arizona, August, 1965.